LHCb Silicon Tracker & Testbeam Data Analysis

- Tracking detectors
- Inner Tracker (and TT) layout
- IT – testbeam analysis
  - Sensor characteristics
  - Cluster properties
  - Inter-strip region
  - HV-scans
- TT-testbeam preparation
LHCb Overview

Tracking detectors:
Inner Tracker Layout

IT: 1.3% of sensitive area
20% of tracks

OT

straw tubes

silicon strip det.

T1 to T3

4.5m

6m

4 layers per station:(2 stereo layers)
⇒ 336 IT modules:
each 168 with 11 and 22cm length
TT-Layout

4 x 1.7m² covered by Silicon strip detectors

376 TT modules

11cm, 22cm and 33cm long
Inner Tracker Modules

Silicon strip detector

Support shelf
Fixation/alignment
Pitch adaptor
Readout hybrid
Balcony

LHCb Silicon Tracker & Testbeam Data Analysis
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Lausanne 03 February 2003
Inner Tracker “Boxes”
Challenges ??? !!!

moderate spatial resolution required (~70µm)
moderate radiation levels 1 Mrad or

\[ 9 \cdot 10^{12} \text{ cm}^{-2} \text{ of 1-MeV neutron equivalent} \]
(e.g. VELO has factor 100 more)

BUT:

minimize readout channels \( \Rightarrow \) large pitch (collect all charges?)
\( \Rightarrow \) large strip length (large noise)
minimize material \( \Rightarrow \) “thin” sensors (little charge produces)
fast readout \( \Rightarrow \) (large noise)
multi-geometry sensors ⇒ find “maximal” pitch
optimize implant width (w/p)

study: S/N, efficiency (inter-strip region)
Test Devices

- Hamamatsu sensors
  - 198 µm and 237.5 µm pitch
  - w/p: 0.25 – 0.35
- Beetle 1.1 at 40MHz
  - read out at 10MHz
- 2 test ladders:
  - short: single sensor
  - long: two sensors
Data Set

- fast and slow shaping
- pulseshape scans
- bias voltage scans 60 – 200 V
- different positions on long ladder
- DAQ timing problem
  ⇒ only “far sensor” usable

All together 23,000,000 events !!
Pedestal and Noise

- no charge calibration ⇒ S/N only
- pedestals and noise are quite stable between runs
  (noise variations between 1.27 – 1.42 observed, indep. of bias voltage)
Clustering & Noise

SeedCut : significance of strips in cluster \( \frac{data^2}{noise^2} \)

\[ \chi^2 : \sum \frac{data^2}{noise^2} \]

• cuts keep noise occupancy below 0.1% with max efficiency
Noise Clusters

correlation in “unassociated” clusters:
sometimes (~15%)
just the track reconstruction failed
Data Quality: some Mysteries

in region A and B (long ladder):
asymmetry w.r.t. strips left and right from track

possible explanations: ADC timing, “echo” on readout
spill over from channel I to channel I+1
corrected: ADC(I+1) = ADC(I+1) – 0.31 ADC(I)
still regarded as not reliable
Data Quality

• large #noise clusters in region E (short ladder)

• low efficiency in region A (short ladder) .. later
Cluster Properties

- charge sharing:
  \[ \eta (x) = \frac{C_R(x)}{C_R(x) + C_L(x)} \]

- “small” region of charge sharing:

- However: up to 15% of the signal in neighbouring strip

<table>
<thead>
<tr>
<th>Voltage</th>
<th>short C</th>
<th>long C</th>
<th>short E</th>
<th>long E</th>
</tr>
</thead>
<tbody>
<tr>
<td>60V</td>
<td>11%</td>
<td>15%</td>
<td>11%</td>
<td>15%</td>
</tr>
<tr>
<td>90V</td>
<td>9%</td>
<td>13%</td>
<td>9%</td>
<td>13%</td>
</tr>
<tr>
<td>140V</td>
<td>8.5%</td>
<td>12%</td>
<td>8.5%</td>
<td>12%</td>
</tr>
<tr>
<td>200V</td>
<td>8%</td>
<td>12%</td>
<td>8%</td>
<td>12%</td>
</tr>
</tbody>
</table>
Cluster Properties

cluster charge: track → 4 neighboring strips
example: region C, long ladder, 90V

16.5% charge is lost between strips
Cluster Properties

charge distribution: Landau × Gaussian

fitted Gaussian widths (3.07 and 3.09) match well(?)

the expectation:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>noise per strip</td>
<td>1.27</td>
</tr>
<tr>
<td>gain variations</td>
<td>0.62</td>
</tr>
<tr>
<td>atomic binding</td>
<td>1.045</td>
</tr>
<tr>
<td>total:</td>
<td>2.83</td>
</tr>
</tbody>
</table>

(of course, dominated by strip noise)
Cluster S/N

S/N normalised to 1 strip clusters:

MPV/Noise (60V-200V runs) \[\Rightarrow S/N = 11.8 - 12.5 \text{ long ladder}
= 15.0 - 15.8 \text{ short ladder}\]

What do we expect?

Beetle 1.1: noise = 870e + 41.5e * \(C_{\text{tot}}/\text{pF}\)
(long ladder: \(C_{\text{tot}} = 34.5\ \text{pF}\) short ladder 17 pF)

MPV: energy deposit in silicon:
90.96 keV in 320 \(\mu\text{m}\) \(\beta\gamma = 120\) (H.Bichsel)
\[\Rightarrow 25127e\]

\[\Rightarrow S/N_{\text{expected}} = 10.9 \text{ long ladder}\]
\[\Rightarrow = 15.9 \text{ short ladder}\]
Impact of the Cluster Algorithm

- cluster finding algorithm:
  - shoulders are not really included
  - mostly 1 and 2 strip clusters

<table>
<thead>
<tr>
<th></th>
<th>reg C, long ladder, 90V</th>
<th>4 strips</th>
<th>after clustering</th>
</tr>
</thead>
<tbody>
<tr>
<td>on strip</td>
<td>15.7</td>
<td>14.2</td>
<td></td>
</tr>
<tr>
<td>between strips</td>
<td>13.1</td>
<td>12.0</td>
<td></td>
</tr>
<tr>
<td>loss</td>
<td>16.5%</td>
<td>15.5%</td>
<td></td>
</tr>
</tbody>
</table>

two strip clusters are found everywhere

relative charge loss remains the same!!
S/N in inter-strip region

example:
long ladder, 90V

slow shaping
fast shaping
Efficiency in inter-strip region

example:
long ladder, 90V
(watch region A,B)

slow shaping
fast shaping

• almost no dip for slow shaping
• 1-2% dip for fast shaping (region C)
Efficiency versus S/N

all HV points + all different track positions →

S/N > 11 → “fully” efficient
HV scan: S/N on strip

slow shaping: higher S/N
slight increase in S/N up to 100V
w/p dependence as expected:

short ladder:
S/N(reg.B) > S/N(reg.C)

long ladder:
S/N(reg.D) > S/N(reg.E)
HV scan: S/N between strips

less increase of S/N between strips with bias voltage than observed for “on strip” clusters
HV scan: “dip” in S/N

dip increases with HV up to 100V

dip is larger for short ladder: because:
same charge loss and lower noise
HV scan: relative dip in S/N relative to the “on strip” S/N, the dip in short and long ladder are of similar size.
HV scan: Efficiency on strip

efficiency is basically constant with bias voltage slightly higher efficiency for slow shaping
HV scan: “dip” in Efficiency

short ladder: no dip
long ladder: dip decreases up to 100V
dip smallest ~1% dip for region C
TT-Testbeam preparation

testbeam period: June 3rd-11th

test “long” TT-modules:

3 LHCb IT–sensors (320µm)
3 GLAST sensors (400µm)
3 CMS sensors (500µm)

test “long” interconnect:
1 Sensor + 55cm Kapton cable
module construction as “test of assembly procedure”: align modules by pushing them against positioning pins.

⇒ accuracy of wafer placement

~ 20µm (250µrad)
(can be improved)
Leakage Currents

Compare leakage currents before (Zuerich) and after gluing (me):

LHCb sensors

GLAST sensors
Leakage Currents

CMS sensors

leakage currents measured to be smaller… some mistake??
Testbeam Summary

• multi-geometry sensors successfully tested
• significant charge loss between strips from previous testbeam confirmed
• charge collection increases up to 100V bias voltage but remains thereafter.
• better charge collection for larger w/p seems to overcompensate increase in noise
• efficiency loss ~3% (237.5 µm pitch) ~1% (198 µm pitch) (long ladder, fast shaping)
• region C is 198 µm pitch will be used in IT (w/p to be decided)
• possible improvements: clustering algorithm, Beetle 1.2, slower shaping time
• work ongoing for TT-related testbeam
Sensor Capacitance

- total strip capacitance: $C_{\text{tot}} = (1.02 + 1.65 \, \text{w/p}) \, \text{pF}$
- region C, long ladder: 34.5 pF
LHCb Overview