The LHCb Vertex Locator

Anne Keune
Ecole Polytechnique Fédérale de Lausanne
The Vertex Locator -VELO- of the LHCb experiment is a precise particle-tracking sub-detector positioned around interaction point 8 of the LHC beams.

The VELO consists of 84 half-moon shaped silicon sensors (paired into modules), arranged in 2 halves along the beam line.

The VELO's main goal is to separate primary and secondary vertices using precise tracking.

Primary vertex resolution: 60 µm (z), 10 µm (x,y)
Proper time resolution: 40 fs (typical value for fully reconstructed B decay)
Sensor Geometry

- Its unique $r\phi$-geometry enables fast impact parameter measurements using 2D $rz$-tracking.

The impact parameter resolution is $14 \, \text{µm}$ for tracks with the highest transverse momentum. The determination of the primary vertex and the IP measurement are used in the 2nd level of the trigger in order to select B decays.

Both R and $\Phi$-sensor contain 2048 readout strips. The R-sensor contains curved concentric strips and the $\Phi$-sensor contains straight radial strips.
Custom-made bellows enable the VELO to retract from its closed position of just 8 mm from the beam line to a distance of 37 mm. This flexibility is used during the commissioning of the beam before it stabilises.

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- The VELO sensors are distanced only 8 mm from the LHC beams.
VELO Vacuum

features

- Its unique rφ-geometry enables fast impact parameter measurements using 2D rz-tracking.
- The VELO sensors are distanced only 8 mm from the LHC beams.
- The VELO is located in a secondary vacuum system within the LHC beam vacuum.

An aluminium sheet of 0.3 mm thick provides a shield between the silicon modules and the primary beam vacuum, with no more than 1 mm leeway to the silicon modules.
In June 2009 the TI8 transfer line from the SPS to the LHC was commissioned. By placing a TED dump before LHCb, splashes of particles went through the detector during the commissioning.

**First results were:**
- more than 50,000 tracks
- VELO sensor timing to ±2 ns
- Module alignment confirmed to ±10 μm in a few hours
- Signal/noise of ~ 22/1
- Track resolution confirmed to ±10 μm in a few hours
- First determination of the separation of the two VELO halves; set to 2 mm in motion system, reconstructed 2.1 mm

*Results are looking very good*
EPFL has developed the off-detector acquisition boards -TELL1s- and its responsibilities range from the transmission of the front-end analogue signal to the firmware implementation of the programmable FPGAs on the TELL1 boards.

The FPGAs perform low level tasks like noise reduction and clustering. The output data of the TELL1 can be zero-suppressed (ZS) which only holds information on the clusters found, non zero-suppressed (NZS) like raw data or both.

16 readout chips (beetles), each processing 128 readout strips

long flexible kapton cables

60 m long analogue data cable
Each beetle processes 128 data strips divided up in 4 analogue links of 32 data strips. The data strips of each link are preceded by 4 header strips.

Beetle readout sequence with the header bits on the left and 4 pulsed channels on the right of about 2 MIPs.
During normal physics running only the ZS output data is sent forward from the TELL1 to the event building network. Therefore it is crucial to verify the ZS algorithm implemented in the FPGAs.

- **Pedestal Subtraction**: Subtracting digitised offset per strip
- **Cross-talk removal and Common mode (CM) suppression**: Noise reductive algorithms accounting for header noise, cable noise and RF pick-up
- **Reordering**: Adjacent strips on the sensor are not necessarily bonded to consecutive beetle channels and therefore need to be reordered.
- **Clustering**: After all noise is suppressed the strips with ADC values above certain thresholds are formed into clusters.
The Emulator

- The emulator reads in the NZS bank and runs the same algorithms in as programmed on the FPGAs, but is programmed in a software environment.

- Using generated NZS data, without tuning the parameters, the ZS output of the TELL1 and the ZS output of the emulation are bit-perfect.

- Using real TED data, there are still some differences between the TELL1 and emulator output (plot). The reasons for this are under investigation.

- Other sub-detectors have been able to verify the FPGA algorithms using TED data.
Conclusions

- A novel rφ vertex detector has been constructed and commissioned in LHCb.
- Pre-processing of the data is performed on programmable FPGAs and the functionality has been verified using generated data.
- First track data results look good and the VELO is ready for the first beam!