The LHCb experiment

The LHCb detector is a single-arm spectrometer which will study the B mesons produced in p-p collisions at the LHC collider at CERN starting from 2007.

**Physical features**

- Luminosity: $L = 2 \times 10^{30} \text{cm}^{-2} \text{s}^{-1}$; $\sim 200 \mu \text{b} \text{s}^{-1}$
- $\sim 100$ events/sec in $\text{d}Q/Q_{\text{cm}}$, CMS
- $\sim 550$ events in $\sim 40 \text{pb}$
- visible events at all level 2 tracks in acceptance
- $\sim 12$ KHz total (visible) interaction rate
- $\sim 10$ MHz total (visible) event rate (pile-up)
- Assumed $\sigma_{\text{ip}} = 500 \mu \text{m}$
- $\sim 200$ KHz event rate
- $10$ KHz: one decay product in the acceptance
- $800$ KHz ce event rate
- But low branching fractions! Expect (offline reconstructable events):
  - $B_{s} \rightarrow \mu^{+}\mu^{-}$ 1 per minute
  - $B_{d} \rightarrow \pi^{+}\pi^{-}$ 1 per second
  - $B_{s} \rightarrow \pi^{0}\pi^{0}$ $\sim 10$ kHz total (visible) event rate (pile-up)

**Global event variables**

- high $E_T$ electrons, photons, $\gamma$
- high $p_T$ muons ($\mu$)
- 'empty' events (HCAL)
- too complicated events (Pile-up+SPD)

**L0-Trigger (L0)**

- Fully synchronous and pipelined hardware trigger (custom electronics) with fixed latency (4 $\mu$s)
- Global event variables ($10$ MHz) to reject:
  - multiple primary vertex (PiP) events, too hard to reconstruct and don't reach the signal content.
  - too complicated events (PiP,SPD)
  - to reduce background from halo-muons;
- B signatures ($780 = 18$ kHz):
  - high $p$ mesons ($\mu$)
  - high E, electrons, photons, $\gamma$
  - and hadrons (HCAL)

**L1-Trigger (L1)**

- Software trigger with maximal latency of $52.4$ ms (max L1-accept rate: $40$ KHz).
- Parallel and overlapping subtriggers:
  - Generic line (to enhance $b$ content)
  - $B_{s}$-Variable: tag (PT)($h_{\text{Og}}$PT), $p_T > 0.15$ mm,
  - Photon and electron lines:
  - $L_{1}$-Variable relaxed ($h_{\text{ecal}}$, $h_{\text{CAL}}$) $3.4$ $\text{GeV}$ ($e$)
  - $L_{1}$-Muons:
    - Single muons, $p_T > 2.3$ GeV, $p_T > 1.5$ mm,
    - Di-muons:
      - $\mu\mu_{m}(\mu_{1}\mu_{2}) < 500$ MeV OR (max 1)
      - $\mu\mu_{m}(\mu_{1}\mu_{2}) > 500$ MeV, $p_T > 0.05$ mm.
- Final decision is OR of all subtriggers

**High Level Trigger (HLT)**

- Software trigger with 2 $\mu$s accept rate.
- Generic HLT: to reduce the rate to 10 KHz, partial reconstruction (IP,PT):
  - $R_{\text{d}}$-Look-alike (with better IP and PT resolution),
  - $R_{\text{d}}$-Look-alike (with better IP and PT resolution),
  - High rate muons ($\mu$ and PT to identify $b$ and $c$),$p_{T}$
  - $R_{\text{d}}$-Specific (to reduce the rate down to 2 KHz), full reconstruction and PID:
    - Fast Inclusive ($1.8$ KHz)
    - easy $\rightarrow$ robust!
    - un-biased sample $\rightarrow$ trigger on the other $B$.
  - for channels uncovered by exclusive selections.
- Exclusive (200 MHz) selections for LHCb hot physics.

**Muon Trigger**

- Straight line search in $M_{2}$-$M_{5}$
- extrapolation to compatible hits in $M_{1}$
- momentum measurement ($\sigma_{p_{T}}$)$\sim 20$% for $b$-decays,
- Sends 2 highest $p_{T}$ muon per quadrant to L0 Decision Unit.

**Level-1 Decision Unit**

- OR of high $E_{T}$ candidates, applies cuts on global variables.

**Conclusions**

While L0 has been finalized and is in production right now, L1 HLT algorithms are still in development. No mass for exclusion in understanding LHCb physical potential.

The final aim is a simple, flexible and robust trigger system, that relies on redundancy (more than one path to trigger an event) for highest possible efficiency.
The LHCb Trigger and Readout

Inside the cavern: L0 electronics
- very high radiation levels (from 1 MeV to 10MeV) around the LHCb detector require radiation hard equipment (rad hard ASICs, stand-alone CPUs but no SRAM based memories);
- each subdetector employs its custom FE electronics;
- only the necessary processing;
- preamplification, digitization (except for the VELO), storing during L0 latency;
- transmission over long cables to the counting house;
- synchronization and timing alignment are major issues.

In the counting house: L1 electronics
- Radiation-safe area, so standard electronics can be used;
- L1 electronics board (see box below);
- L1 processing takes place in the counting house;
- data received from various FE cards;
- finds electrons, photons, hadrons and muons candidates. 
- for the calorimeters trigger, the TELL1 board is used.

General electronics architecture:
For each trigger level, it consists of:
- some data processing (digitization, zero-suppression);
- a buffer defined by the trigger latency;
- an output buffer to communicate the data transmission to the next trigger level;
- an interface to receive the trigger decision.

Electronics requirements
- L0 and L1 latency
- Variable (max ~ 1ms, min ~ 8μs)
- Maximum output rate
- 1.1 MHz
- 40 MHz
- Buffer size (evts)
- 160
- 58254
- Board dimensions
- 16 x16 cm2
- 2 METs

The TELL1 readout board
The TELL1 is an FPGA based board made to readout the data accepted by the L0 trigger and output them, after some processing, to L1 and HLT. It will be used by all LHCb subdetectors but the RICH (see brown box on the right). Specific detector needs are accomplished by mezzanine cards while FPGAs allow the necessary flexibility for different data processing. Advantages of having a common board are the reduced development and maintenance costs, and software reuse for all common interfaces.

TELL1 dataflow
TELL1 accepts L0 accepted data as input. After a first synchronisation, the dataflow is split. For the L1 data path, zero suppression is applied and processed data are sent to the L1 PC farm. For the HLT data path, raw data are stored in the L1 buffer and, if the event is accepted, zero suppressed and sent to HLT. The interface to the event building network is provided by four Gigabit Ethernet links.

L0 data input
- Veto on the link (14-15)
- Variable (max ~ 1ms, min ~ 8μs)
- Maximum output rate
- 1.1 MHz
- 40 MHz
- Buffer size (evts)
- 160
- 58254
- Board dimensions
- 16 x16 cm2
- 2 METs

L0 & HLT PC farm
- Both L1 and HLT algorithms are executed on the same level of commercial PC.
- They share:
  - Ethernet network;
  - Sub-farm controllers;
  - Computing nodes;
- It is flexible and scalable.
- L1 bandwidth: 40 Gbps
- HLT reconstruction runs in background.
- CPU share:
  - L1 = 90%
  - HLT = 10%
  - Reconstruction = 20%

The Rich readout board
Compared to 'standard' TELL1 readout, the Rich readout board:
- does not foresee L0 trigger interface;
- binary readout: more input channels → less processing power needed.
- The Rich readout board will however all requested functionalities to fill into LHCb subdetectors.
- reads data from detectors, from up to 48 optical links, de-serialises, zero-suppresses, mixes and can be adjusted for optimal packet size to tune the network traffic.

Real Time Trigger Challenge (RTTC)
- Why?
  - Test one (or few) subflavors of the DAQ under realistic conditions:
  - Fast data path (from detector to producer)
  - In width: more detector cards
  - Test realistic L0/L1/HLT code
  - Measure realistic overheads
  - Performance testing
  - Modern CPUs compared to today's standard CERN PC.
  - Test controlling: Monitoring, conditions DB, Farm control, etc.

- What?
  - One (or few) racks of 4 CPUs
  - 2 Sub Farm Controllers (SFC)
  - TTC data (one disk server for input/one for storage):
  - 2-4 Sub Farm Controllers (SFC)
  - 10 Level-0 YES, 400k Level-1 YES events, 20k HLT yes
  - Measure realistic overheads
  - Test realistic Level-1/HLT code
  - Test controlling: Monitoring, conditions DB, Farm control, etc.
  - Start: June - July 2005
  - End: June - July 2005

NOW!!