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The LHCb trigger and readout[1]

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Abstract

We give a brief overview of the LHCb readout scheme and trigger strategy. The latter is based on three levels designed to reduce the event rate from 40 MHz to 2 kHz.

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Contents

1 Introduction

The LHCb detector is a single arm spectrometer designed to exploit the large $b\bar{b}$ cross section at the LHC, in order to make precision measurements of CP violation and rare decays in the B sector. The LHCb experiment plans to operate at an average luminosity of 2×10^{32} cm^{-2}s^{-1}, while the LHC bunch crossing rate is 40 MHz [1]. The low luminosity and the LHC bunch structure will provide about 10 MHz of interactions visible to the LHCb detector, which will contain a rate of $b\bar{b}$ pairs of the order of 100 kHz. However, only 15% of these events contain at least one B-meson with all its decay products in the acceptance. Furthermore, the final states useful to study CP violation have typical branching fractions below 10^{-3}. Hence the task of the trigger system consists in reducing the initial 10 MHz rate to a few kHz, at which rate the events can be written to permanent storage, while maintaining the highest possible efficiency for the decay channels of interest for CP violation studies [2]. This reduction is achieved in three trigger levels: the L0 trigger, which is implemented in custom electronics, will reduce the acquisition rate from the initial 40 MHz down to 1 MHz; the L1 trigger will accept events at a rate of 40 kHz, while the HLT will further reduce the rate down to 2 kHz in the present implementation. Both the L1 and HLT algorithms will be executed on a dedicated PC farm (about 1600 CPUs).

In the next Section we present the current implementation of the readout system, while in Section 3 we briefly discuss the trigger strategies.

2 Readout system and trigger architecture

The LHCb spectrometer and all its subsystems are fully described in [3], and major updates and modifications are reported in [1]. A detailed scheme of the Data Acquisition (DAQ) system is shown in Fig. 1; for a complete description of the readout scheme we refer to [2]. The architecture of each trigger level is straight-forward: it consists of some data processing (preamplification, digitization, zero-suppression), a buffer to store raw data (the size of which is defined by the trigger latency), an output buffer to derandomize the data transmission to the next trigger level, and an interface to receive the trigger decision.

The LHC environment will be quite harsh in terms of radiation exposure, requiring the use of full custom electronics in the proximity of the detectors. To cope with the high event rate and data bandwidth, however, most of the data processing will be done with standard electronics in the counting house behind a shielding wall. Thus synchronization and timing are essential issues for a correct readout. LHCb will have both a fast Timing and Trigger Control (TTC) system to distribute the LHC clock, resets and triggers [4], and a slow Experiment Control System (ECS), responsible for configuration, control and monitoring of all online components [5]. Synchronization and scheduling of trigger decisions are accomplished by the Readout Supervisor (RS) [6].

The L0 electronics, i.e. the DAQ components before the L0 decision, will be

located in the LHCb cavern, and its implementation is specific to each subdetector. The L0 decision unit, which receives data from the various L0 trigger processors and delivers the L0 decision to the RS, is located in the counting house. The L0 is a fully synchronous and pipelined hardware trigger with a fixed latency of 4 μs, which gives a buffer depth of 160 events. The front-end is required to readout events in 900 ns, hence the maximal L0 accept rate is 1.11 MHz.

The L1 electronics, i.e. what comes before the L1 decision, is implemented with standard electronics, since it is entirely situated in the counting house, where data are sent to over long (50–100 m) analog or digital links from the L0 electronics. The L1 is a variable latency trigger with a buffer size of 58524 events, which combined with the minimal events spacing of 900 ns and the requirement to deliver the decisions chronologically allows a latency up to 52.4 ms. All LHCb subdetectors but the RICH have chosen the TELL1 board [7] as a common solution for the L1 readout. The TELL1 is an FPGA based board designed to take as input L0 accepted data and, after some processing specific to each subdetector, to output them to the L1 and HLT readout network, which is based on standard GigaBit Ethernet.

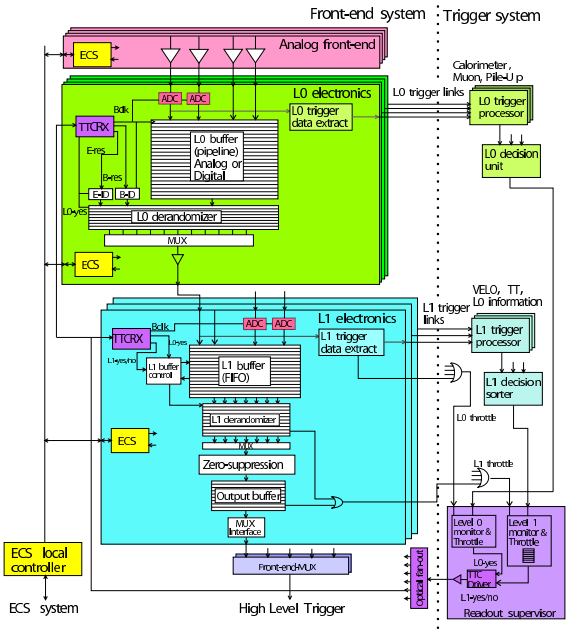

Figure 1: The LHCb front-end trigger architecture.

3 The trigger strategies

The LHCb trigger system is fully described in [2]. Here we give a short summary of the various trigger algorithms and an update on their performances. In Table 1, the b and c content in generated events after each trigger level is shown.

The objective of the *L0 trigger* is to reduce the acquisition rate so that all subdetectors data can be digitized and stored in the L1 buffer. L0 exploits the large

mass of b hadrons, looking for events with large transverse energy deposition in the calorimeters and in the muon chambers. It also features a Pile-Up system to reject events with multiple interactions. The achieved efficiencies vary from as high as 90% for channels with dimuons in the final states to about 50% for hadronic channels.

The *L1 trigger* consists of a set of parallel algorithms, whose individual decisions provide the input to a logical OR giving the final decision. A generic trigger line enhances the b content by selecting events containing tracks with both high transverse momentum and large impact parameter, whereas some specific lines select final states with electrons, photons and muons. The inclusive muon line is particularly important in order to have an unbiased sample to use for life times sensitivity studies. The efficiencies are around 80% for purely hadronic channels, and about 90% for channels with dimuons.

The *High Level trigger* algorithms can be divided in two parts. In the first, generic part, the L1 decision is reconfirmed, and a fast muon identification is performed. In the second, specific part, an inclusive stream of muons and D^* events is formed, which covers about 1.8 kHz of the available bandwidth, while the remaining 200 Hz are reserved to the exclusive selection of some core channels of the LHCb physics programme. Preliminary results show efficiencies of the order of 95% for dimuon channels, and around 90% for channels with two hadrons in the final state.

Table 1: Rates of crossings with at least one bottom ($b\bar{b}$), and if no bottom at least one charm ($c\bar{c}$), in generated minimum-bias events after each trigger level.

	$b\bar{b}$ (kHz)	$c\bar{c}$ (kHz)
Generated	165	840
After L0	30	106
After L1	6.4	7.2
After HLT generic	3.8	2.7

4 Conclusions

We have presented an overview of the present implementation of the LHCb trigger and readout scheme. Most of the electronics components are being delivered and tested in these months. The L0 trigger performance is quite stable, while L1 and HLT algorithms are still being optimized. A dedicated "Real Time Trigger Challenge" has been successfully setup and run in July 2005 to test the online environment under realistic data taking conditions, such as full-speed data path (from simulated detector output to storage) and long term operation (hours).

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