LHCb

Test of VELO detector FE chips using the ODE-PP

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Abstract

A test system for the SCTA-128 FE chip has been assembled using the RB2 prototype of the Digitizer board. The main feature of the system is the capability to exploit the 40 MHz read-out of SCTA-128 FE chip using RB2 FADC cards. This note describes the components of the test system. Hybrids mounted with SCTA-128 are characterised. Data obtained from an Hamamatsu silicon detector used during summer 2000 VELO test beam allows a comparison between the RB2 FADC performance and the results from the test-beam data acquisition system.

Document Status Sheet

Table 1 Document Status Sheet

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1 Introduction

The setup of a test system for the SCTA-128[1] chip which makes use of the L1 Digitizer board prototype RB2[2] was motivated by two main reasons.

One reason was to test the FE chips. In the summer 2000 VELO test-beam, the prototype sensors were equipped with SCTA-128 FE chips. The SCTA-128 chips used were not tested by the manufacturer and a test system which is able to characterize the chip before the detector assembly was therefore required. The RB2 can be used as a data acquisition board for the test setup as it is capable of sampling the output sequence of SCTA-128 at 40 MSample/s.

The other reason was to test the FADC card in the RB2 board. The SCTA-128 chip is very similar to a possible future VELO FE chip[3]. In particular, the SCTA-128 output after a L0 trigger command is issued consists of an analog sequence of the sampled channels with a rate that can be varied from 5 MHz to 40 MHz. The VELO custom L1 electronics has to digitize the analog data streams coming from FE chips in the L0 electronics. This will be done by the RB2 digitizer prototype which carries up to two Flash ADC (FADC) daughter cards. The SCTA-128 chip can be used to test the performance of the FADC cards.

2 Test system overview

The test system is composed of three VME boards, which will be discussed in detail in the following sections:

- The sequencer (SEQSI) provides clock and sequences of commands to the FE chips.
- The trigger generator (TTCvi) generates the optical signal that encodes the clock and the trigger command for the RB2.
- The RB2 digitizes and stores data.

The input and output signals to the FE chips are routed through a Repeater Board. Figure 1 shows a schematic view of read-out system.

All the boards use the SEQSI 40 MHz clock: in particular, data acquisition in RB2 is in phase with the clock of the FE chips. The data acquisition is triggered by a VME trigger command to the TTCvi board. The trigger signal is routed to both SEQSI (as a NIM signal) and RB2 (as encoded optical command). At the trigger the SEQSI issues a LV1 accept command sequence to the FE chips while the RB2 starts to digitize data and to store them into internal FIFOs.

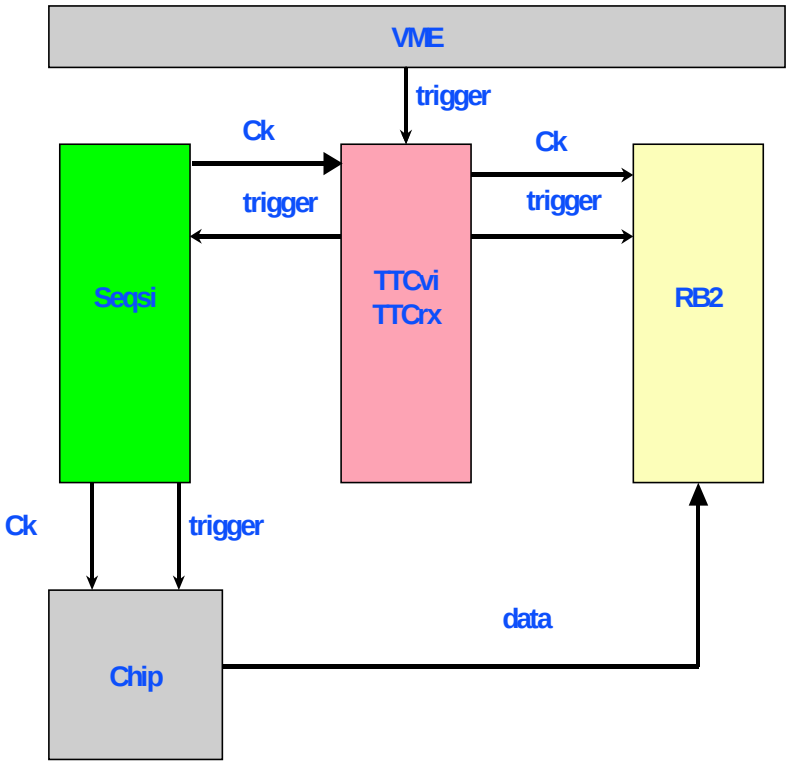

Figure 1 Schematic view of test system.

2.1 Repeater board

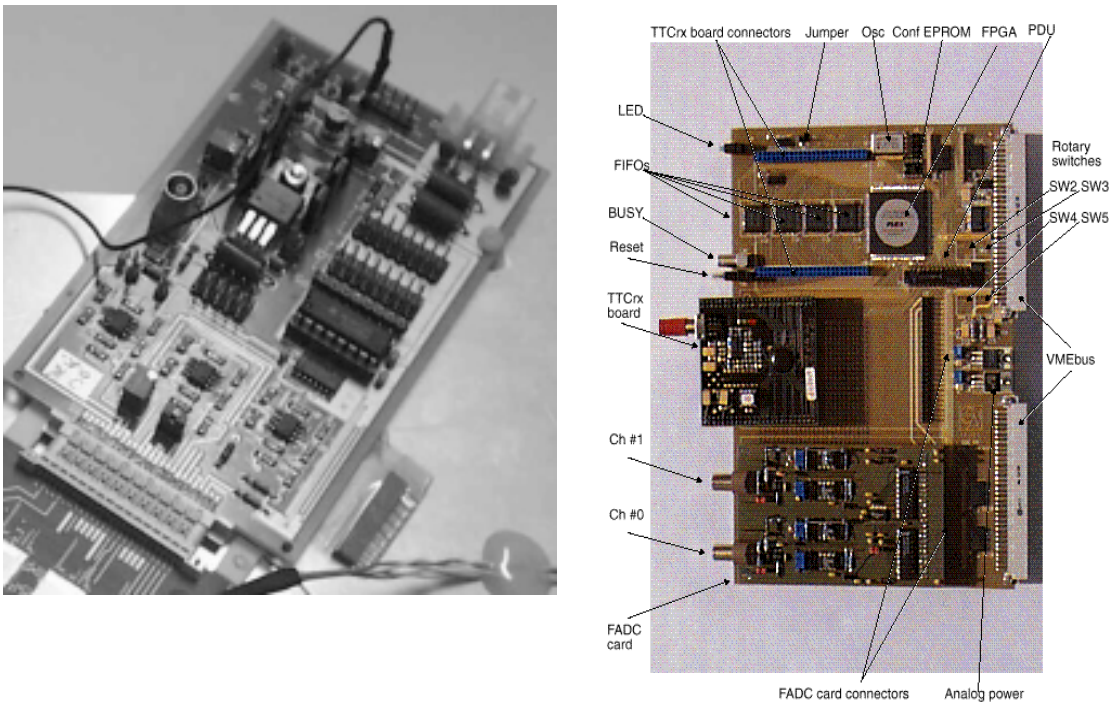

Figure 2 Left: photograph of the repeater board. The connector to the ceramic hybrid equipped with FE chip can be seen in the bottom left corner. Right: the RB2 board.

The Repeater Board used in the test system is shown in Figure 2.

The board supplies the analog and digital voltage to the FE chip, and the reference voltage Vref. The value of Vref, as well as the analog and digital voltage, can be varied acting on a variable resistance and tested on a probe pin.

The board translates the input commands (including the L1 accept), the reset and the clock from ECL to LVDS and routes them to the hybrid. Probe pins allows the signals to be monitored.

The board provides line drivers that convert the analog FE chip output to a bipolar signal. It is possible to shift the signal baseline using a variable resistance on the board, in order to adjust the channel pedestal level to within the FADC dynamic range.

2.2 Read-out board (RB2)

A detailed description of the RB2 (Figure 2) can be found in [2].

In the test system the RB2 board is operated in mode 0. In this mode the read-out sequence is triggered by an external trigger command and consists of 2048 sampling commands at 40 MHz rate to the FADC cards. The RB2 memory at the end of read-out sequence contains the 2048 samples. The memory is then accessed by a VME command and processed by the acquisition software in order to extract the charge information for each channel.

The RB2 used in the test setup makes use of the clock signal decoded by the TTCrx daughter card. The TTCrx decodes also the trigger signal.

It is possible to set, with the resolution of 1 ns, the skew between the RB2 clock and the sampling clock issued to the FADC cards via a VME command. The skew value can be varied to optimise the sampling of the input signal.

2.2.1 Fast ADC daughter board (FADC)

The SCTA-128 output signal dynamic range is 700 mV. In the FADC card the bipolar signal from the Repeater Board is converted back to the original SCTA-128 output signal. The gain of the total amplifier chain is set to 1. The output signal is added to a constant offset of 2 V, i.e. the FADC card 8-bit ADC chip AD9059 digitizes signal in the 2V - 3V range. The ADC conversion factor is 1V/256 = 3.90 mV/adc count. The ADC intrinsic resolution is 0.28 adc counts, or 1.1 mV. The ADC linearity has been measured[4], using a voltage generator, to hold for the full ADC range. The measured voltage turned out to vary between samplings with a RMS up to 0.5 ADC counts. The RMS was found to depend on the voltage value.

2.3 TTC-VI and TTC-VX boards

In the test setup the RB2 clock and trigger command is issued by the VME boards TTCvi and TTCvx[5]. The TTCvi is used in VME trigger mode: the trigger command is issued by a VME command; the command is sent at the same time to the SEQSI through a NIM output and to the RB2 via the optical fibre as a trigger command to the TTCrx chip, encoded in the 40 MHz clock. The TTC-VI and TTC-VX system 40 MHz clock is provided by the SEQSI. The trigger command is synchronized with the system clock.

2.4 SEQSI SCTA sequencer

The SEQSI[6] is a VME board which provides a programmable sequence of ECL signals at 40 MBit / s. Three ECL signals are sent to the SCTA-128 chip: the clock at 40 MHz, the reset (active low) and the command. Of the many features of the SEQSI board, the test setup uses the capability to provide a 40 MHz clock (used as the master clock of the system) and the capability to loop over an idle sequence and to switch to a data acquisition sequence when an external trigger is sent. The external asynchronous trigger is latched with the SEQSI master clock.

2.5 Data Acquisition Software

The test setup VME controller is a CES RIO 8061, PowerPC 604 which uses the LynxOS real-time operating system. The OS maps the VME registers into the RIO memory, so the user can access the board registers by functions coded in C.

The Data Acquisition software consists of utility functions collected into libraries and executable code. There is one header file which declares functions used to configure and control the RB2 (ode.h), one header file to configure and control the TTC-VI board (TTCvi.h) and one header file to configure and control the SEQSI (seqsi.h). Additional libraries (Module.h and scta.h) include functions that are used to build up the sequences of commands to the SCTA-128 chip. The executable code includes: a program which issues random triggers, used to measure the channel pedestals (pedestal.c); a program which issues the test pulse command to the chip, used to measure the channel gain by injecting a programmable charge into selected channels (gain.c); a program which combines the two previous features to perform a complete test of a chip in the hybrid (hybrid_test.c).

Amongst the RB2 functions, `ODERead()` is of particular interest. This function returns a list of ADC values for each channel. The function algorithm is the following: first the memory location where the beginning of the data is recorded is found; then the memory locations are copied into a channel value array. The trailer and header information is skipped. `ODERead()` knows the read-out speed of the SCTA-128 and hence skips the required channels when the chip is read at 5, 10 and 20 MHz. An optional median filter can be applied to the data, which reduces the effect of common oscillation of the channel ADC values.

The program flow is basically the same for all the programs mentioned above. First, the boards are initialized; then the trigger VME command is issued to the TTC-VI board. The TTC-VI sends at the same moment the trigger to the RB2 and to the SEQSI. The RB2 starts sampling the input values from the SCTA-128 and stops when the 2048 locations of the internal memory are full. The SEQSI address memory pointer jumps to the location specified by the trigger register and starts out putting the sequence of programmed commands. In the case of the pedestal.c program the command sequence consists only of the trigger command; in the case of gain.c the command sequence contains the commands to set the SCTA-128 internal pulse value, the inject pulse command and the trigger command. The data on RB2 are then read and the channel ADC values are written in an ASCII file for subsequent analysis or used to obtain an online measurement of the pedestals and the gain.

3 SCTA characterisation

The test system described above has been used to characterize the SCTA-128 chips used in the summer 2000 test-beam.

3.1 The prototypes

The SCTA-128 chips have been glued to ceramic hybrids. Two different kinds of ceramic hybrids have been produced: SCT3 and SCT6. SCT3 can be equipped with up to three SCTA-128, while SCT6 can be equipped with up to six. In the SCT3 two of the three chips are read-out in a daisy chain, while one is read-out on its own. In the SCT6 all chips are read-out in daisy chain. Figure 3 shows the numbering scheme for chips on SCT3 and SCT6 hybrids,

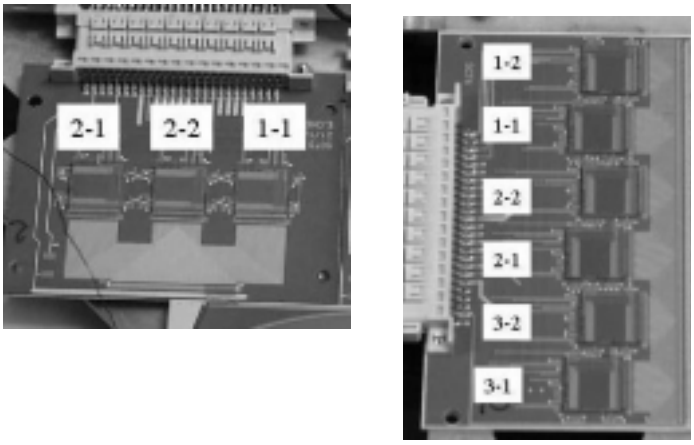

Figure 3 SCT3 and SCT6 hybrids equipped with chips.

following the sequence in which they are read out.

A total of five SCT3 hybrids and two SCT6 hybrids has been fully equipped and tested. Some hybrids have been reworked in order to replace non-working chips. In Table 2 the existing hybrids are summarized together with the sensor prototypes they equipped.

Table 2 Summary of hybrid production.

Hybrid tag	Detector mounted	N. of mounted FE's	N. of replaced FE's
SCT3_1	MICRON PR02-PHI[7] (irradiated region)	3	0
SCT3_2	HAMAMATSU PR01-PHI (unirradiated region)	3	0
SCT3_3	none	3	0

Table 2 Summary of hybrid production.

Hybrid tag	Detector mounted	N. of mounted FE's	N. of replaced FE's
SCT3_4	MICRON PR02-PHI (irradiated region).	3	2
SCT3_5	HAMAMATSU PR01-PHI (irradiated region).	3	2
SCT6_1	none	6	0
SCT6_2	"FAST STATION" (unirradiated HAMAMATSU PR01-R[8])	6	2

3.2 Pedestals

The pedestal linearity and spread has been measured for all the chips. Figure 4 shows the pedestal distribution for a typical chip. The pedestal distribution is in most of the chips flat: the only exception is chip SCT3_4_1_1 (Figure 5) which showed a pedestal dependency on channel number. The pedestal spread for this chip after median filter was comparable to the one of the other chips.

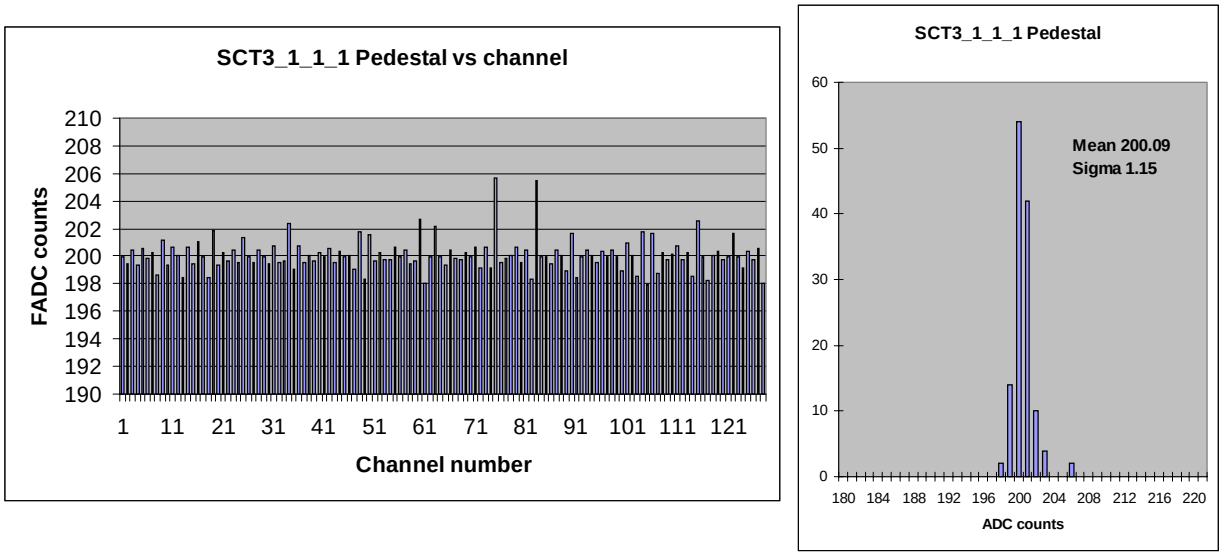

Figure 4 Left: SCT3_1 single-read chip pedestals. Right: pedestal distribution.

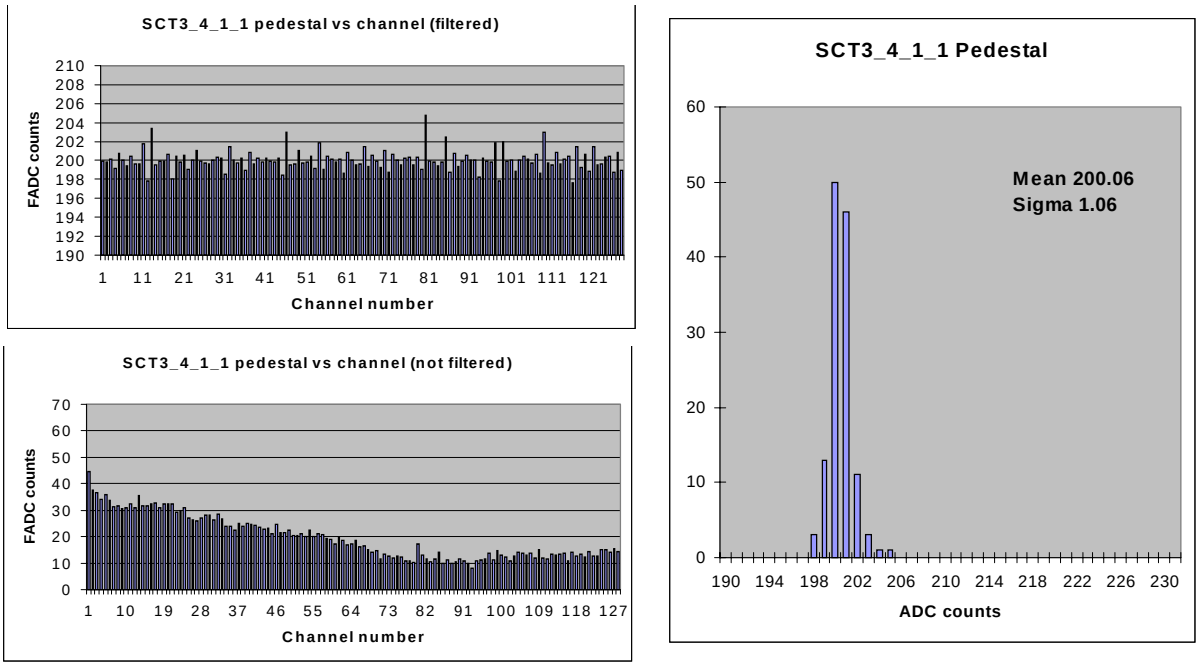

Figure 5 Upper Left: SCT3_4_1_1 pedestal vs. channel number after median filter. Lower Left: SCT3_4_1_1 pedestal vs. channel number before median filter. Right: SCT3_4_1_1 pedestal distribution after the median filter

3.3 Noise

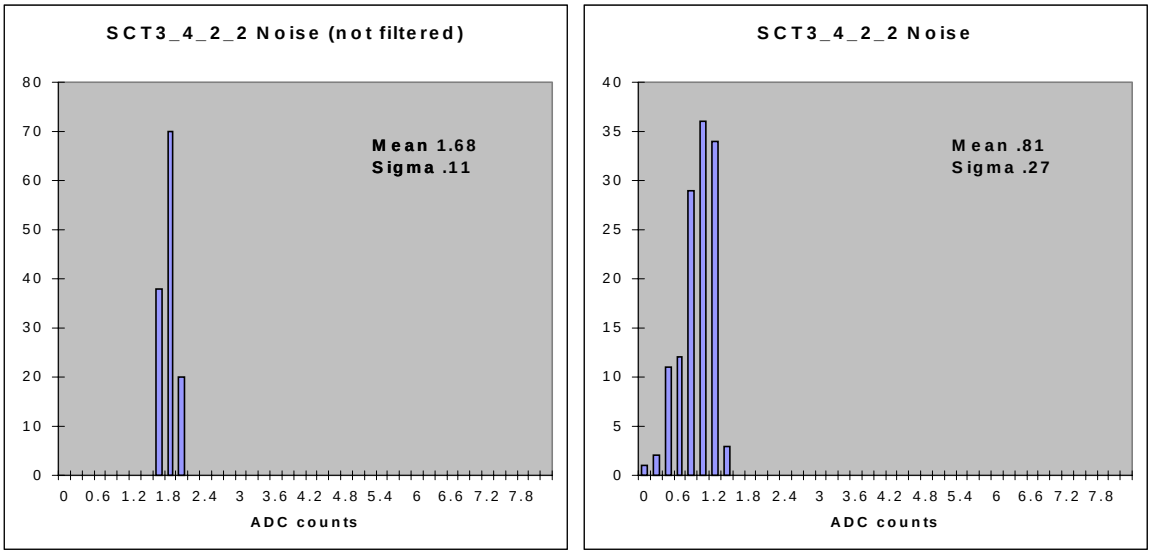

Figure 6 Left: Noise in adc counts for SCTA-128; Right: the same chip, but data are corrected by the median filter.

The channel noise is defined as the RMS of the pedestals. A median filter can be applied to the data: the effect is to reduce the RMS. Figure 6 shows the effect of the median filter on the noise measured in one SCTA-128 chip (SCT3_4_2_2).

3.4 Gain

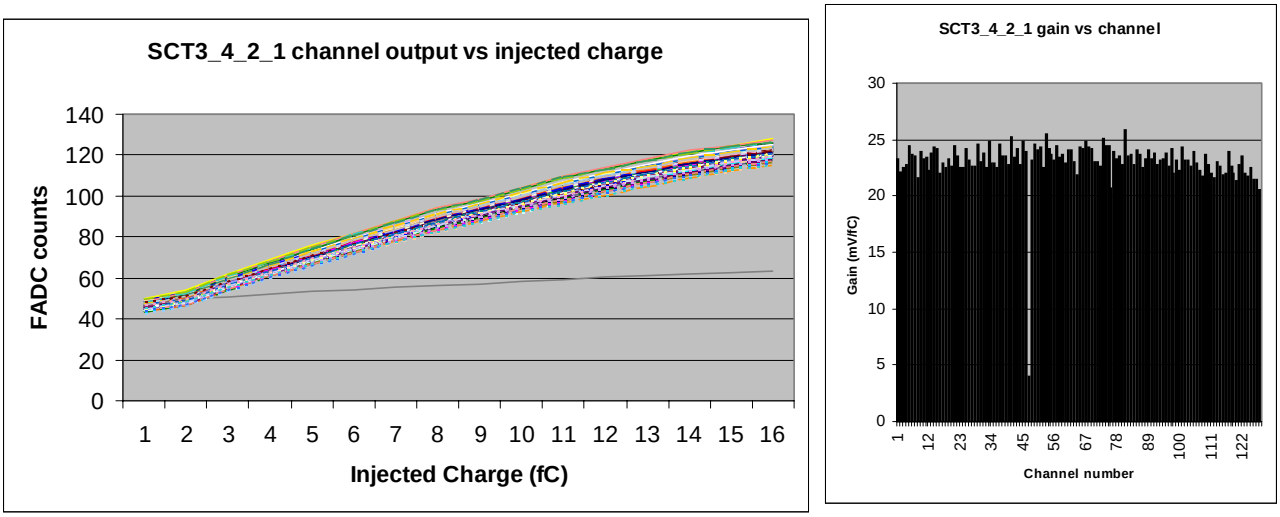

Figure 7 Left: Channel output as function of the injected charge. Each channel is represented by a line. Right: Gain distribution.

The SCTA128 internal injection circuit has been used to pulse the preamplifier. Figure 7 shows the channel output as a function of the injected charge. For large charges the gain tends to be smaller. However there is a good linearity up to an injected charge of ~12 fC, a value that exceeds the typical 4 fC charge released by one MIP.

The gain is defined as the ratio between the injected charge and the channel output. Since the gain is only approximately linear, we have to choose a value of the injected charge at which we compute the gain. We choose a value of 7 fC, where the gain is still linear but above the charge released by one MIP.

The typical measured gain value is of the order of 20 mV/fC. The gain uniformity and the number of dead channels varies from chip to chip.

Figure 8 shows the gain vs. channel number for a good quality chip and for a chip with many missing channels and a lower mean gain.

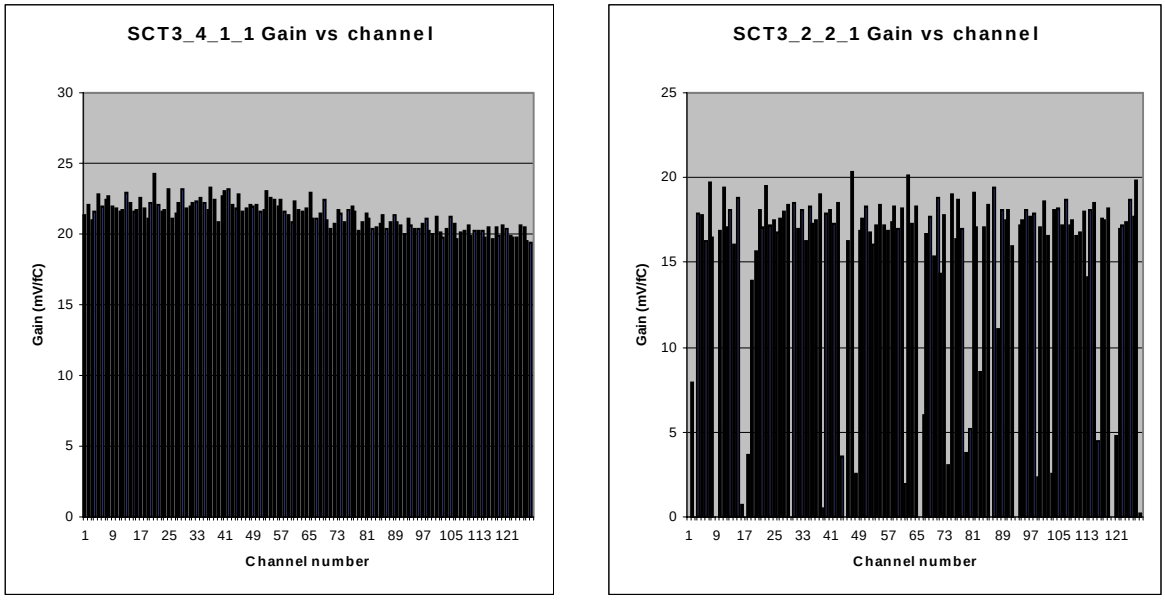

Figure 8 Left: gain vs. channel number for a good chip(SCT3_4_1_1). Right: a bad chip that has a large fraction of channels with low or no gain (SCT3_2_2_1)).

3.5 Hybrid test results

The complete noise, pedestal and gain results for the produced hybrids are given in full detail in [9]. According to the test results the FE chips have been divided into three categories:

- **Gold**

  Chips with uniform gain of the order of 20 mV / fC with no or few dead channels, pedestal spread of less than 5 ADC counts and mean noise of the order of 1 ADC count.

- **Silver**

  Chips that, although not satisfying all the above requirements for all channels, have a subset of channels with “gold” characteristics and therefore are still useful to equip detectors.

- **Bad**

  Chips that fail to meet the gold or silver requirements. In this category we include also the defective chips which we replaced on the hybrid.

Those quality criteria (although not strict) have been used to make a selection on hybrids to equip the detectors. Table 3 summarizes the results of the chip tests for the produced hybrids.

Table 3 Summary of chip test results.

Hybrid code	"gold" FEs	"silver" FEs	"bad" FEs	unknown[a]
SCT3_1	3	0	0	0
SCT3_2	0	1	2	0
SCT3_3	0	1	2	0
SCT3_4	2	1	2	0
SCT3_5	2	0	3	0
SCT6_2	4	2	2	0
SCT6_1	0	0	0	6

a. "unknown" chips are chips that have not been bonded and/or tested.

If we define the chip yield as the ratio between the amount of gold chips and the sum of the tested chips we obtain a yield value of ~ 40%.

4 Test of a VELO silicon sensor equipped with 6 SCTA-128 chip read-out

The Hamamatsu PR01-R 300 μm thick detector ("fast station") used in the summer 2000 test-beam has been tested in our test setup. The characterization of the FE chips which equip the detector allows a comparison of the performance of the two systems. Moreover it is possible to obtain an absolute calibration of the FADC cards using test-beam data.

From the test-beam data measurements a value of 58 ADC counts as the most probable value of the charge Landau distribution for a MIP has been obtained[8]. A CAEN C-RAMS 10-bit ADC V550[10] was used in test-beam, with sensitivity range of 1.5 V, that implies a conversion factor of 1.5 mV/ADC count. Assuming that the most probable value of the Landau corresponds to 22000 e- we obtain a conversion factor of 252 e-/mV. In terms of ADC counts, we have the following conversion factors: for the FADC card, 983 e-/ADC count; for the C-RAMS, 378 e-/ADC count.

4.1 Analysis Software

The data taken with the detector test set-up in the VELO Lab are analysed in a very similar manner to the test-beam data[7].

In the first step, data from the SCTA are written to an ASCII file. This is then converted to an FZ file, with the file format being fully compatible with the standard test-beam software as described in [11]. Therefore the same class structures and analysis routines, such as the description of the bonding patterns of detectors, the calculation of noise and the common mode suppression (CMS) algorithm are used in the lab tests of a single detector as are used in the full test-beam. This allows a direct comparison of the results, excluding the possibility that a disagreement of lab and test-beam results could be caused by differences in the analysis software and allowing the exploitation of common useful features.

The key element of the conversion of lab data to the test-beam format is the program `Fz_ConvertLab`. As input it takes two files. First is the ASCII file, containing an overall header, and for each event the raw ADC data itself. The second is a configuration file, which again is of the same type as used in the standard test-beam analysis. The main output of `Fz_ConvertLab` is an FZ file, matching the detectors specified in the configuration file. In it, SCTA chips for which data are not present in the ASCII file are filled with a default ADC value. This can be necessary e.g. when a detector with a six-chip hybrid is tested in the lab, and only two chips are read-out.

Furthermore, there are conceptual differences between the lab tests and the test-beam data. For example, in the test-beam one usually tries to reconstruct tracks, whereas for a lab test the emphasis is more on studying the detector noise or the chip gain. One can also verify if a chip works properly. This means that some analysis functions have been defined which can only be meaningfully called for lab test data. A typical example is the `gainscan()` analysis function, which can be called when a predefined charge between 0 and 16 fC is injected in every fourth SCTA channel.

4.1.1 Hybrid measurements

With this software we tested a hybrid equipped with one SCTA-128 chip with no capacitive load. Pedestals and noise have been measured. The pedestal spread is 1.14 ADC counts, in agreement with the results obtained with the online software described in Section 2.5 (Figure 9).

The noise measurement is shown in Figure 10. The beneficial effect of the CMS algorithm applied to the data is clearly visible. The mean value of the measured noise is reduced from ~ 1250 e- to ~ 840 e- after common mode correction. The measured noise and the effect of the common noise suppression are of the order of what was measured in other hybrids with the online software.

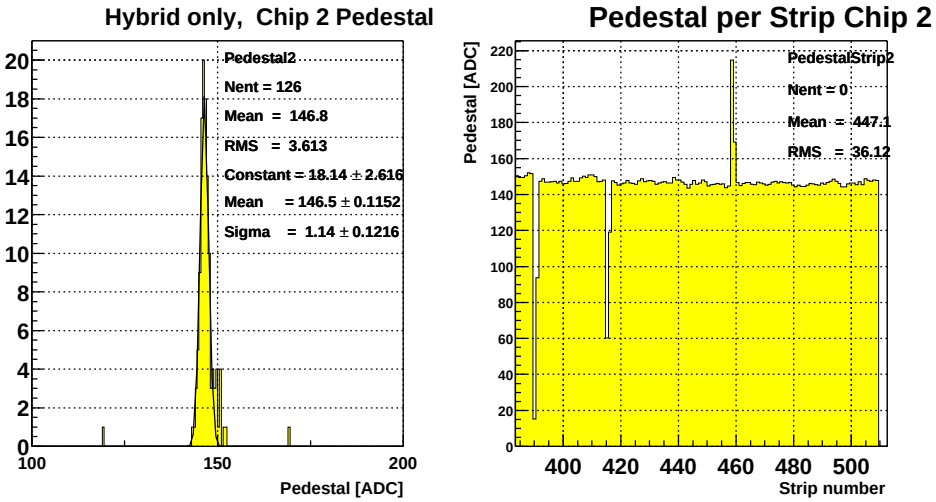

Figure 9 Pedestal for a SCTA-128 chip with no load capacitance.

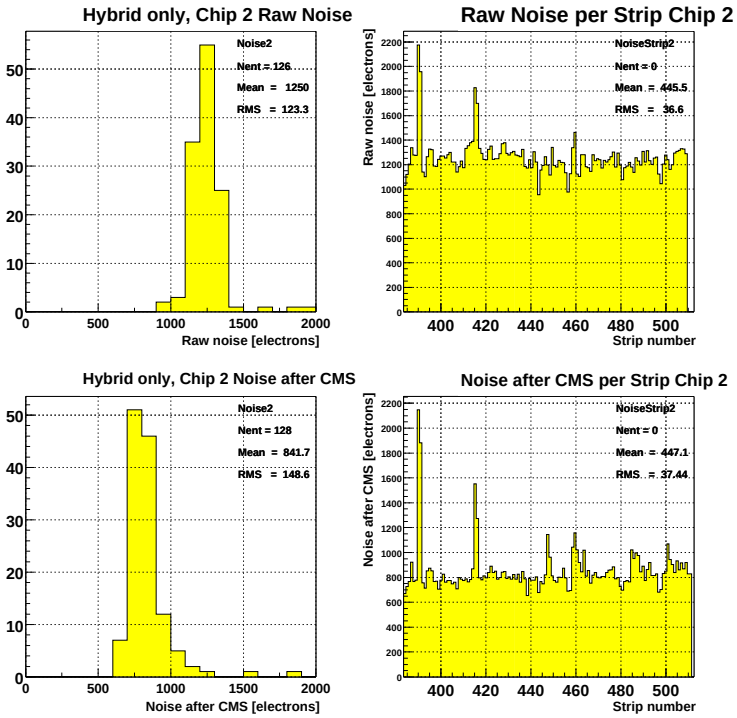

Figure 10 ENC in electrons before and after common mode correction for a chip with no capacitive load.

4.2 System setup

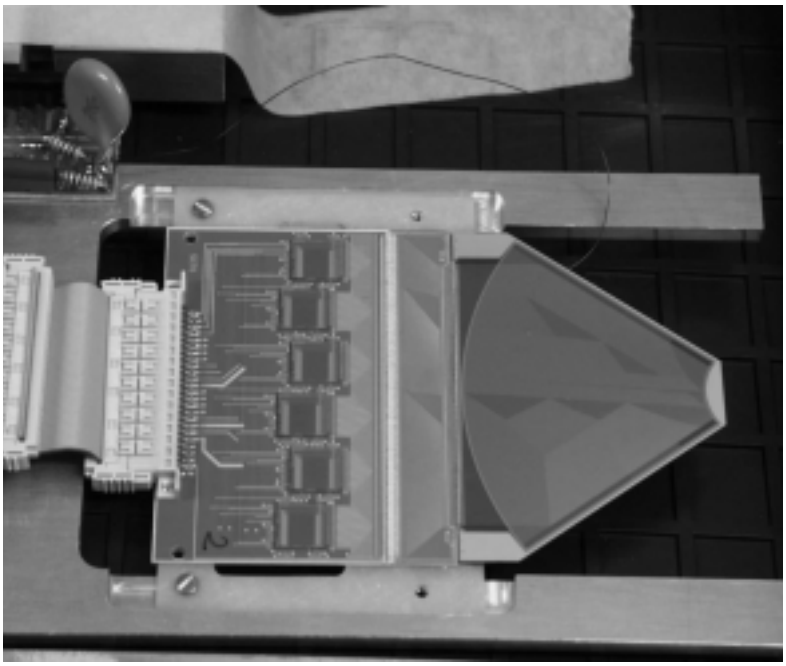

Figure 11 Hamamatsu PR01-R detector (“Fast Station”)

Figure 11 shows the detector and the SCT6 hybrid with the FE chips. The chips used in the laboratory measurements are 2_1 and 2_2. Those chips are connected to regions of the detector with different capacitance due to the different strip and routing lines lengths. In [12] a measurement of the capacitive load for PR01-R detector is reported: a value of about 15.5 pF is expected for chip 2_2, while for the chip 2_1 the capacitive load is expected to be between about 22 to 23 pF. The effect, as seen in test-beam data, is to increase the noise in chip 2_1 which is connected to the longer strips. In the remainder of this note the chip 2_1 will be “chip 1” and the chip 2_2 will be “chip 2”, while in the standard test-beam analysis those chips are referred to as “SCTA 3” and “SCTA 4”[8].

4.3 Measurements

Except where is explicitly noted, all measurements on the fast station have been done with the following settings:

- The preamplifier current is 200 μA, the shaper current is 40 μA, the read-out amplifier current is 70 μA.
- The silicon sensor is reverse-biased at 90 V.
- The read-out speed of SCTA-128 is 40 MHz.

4.3.1 Noise

Noise measurements in laboratory are of particular interest since the noise measurements in the test-beam have been performed with the SCTA-128 read-out at 5 MHz, while the laboratory measurements are done at 40 MHz rate as will be the case for the final VELO.

Figure 12 shows the noise vs. the channel number for the two central chips of the fast station before and after CMS. The noise shows a dependency on the channel number, which can be

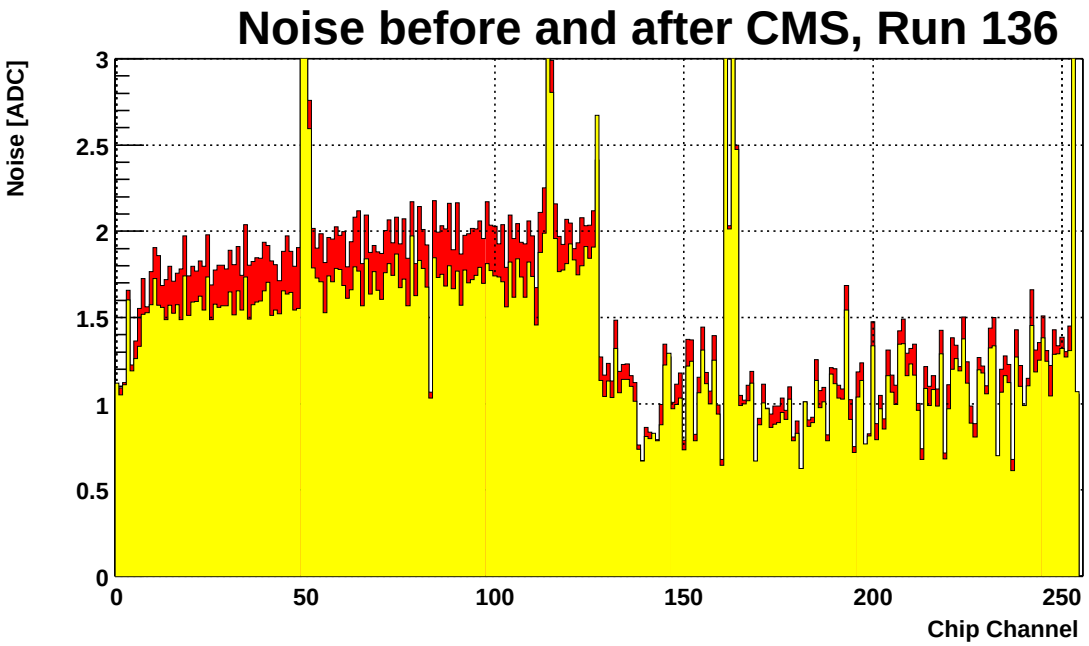

Figure 12 Noise vs. channel number for the “fast station” before (dark) and after (light) common noise suppression.

mapped into a dependency on the capacitive load which increases with channel number for chip 1, while it is somewhat more constant in chip 2. Channels in the range 0 to 127 are bonded to strips of 3.5 - 4.5 cm length, while those in the range 128 to 256 are bonded to 0.6 - 0.8 cm long strips. The mean ENC is 1646 e- (1033 e-) for chip 1 (chip 2).

Figure 13 shows the noise as a function of the channel number for the same detector, as measured in a typical test-beam run. The noise value is in ADC count: the corresponding mean ENC value is about 1600 e- (1100 e-) for chip 1 (chip 2).

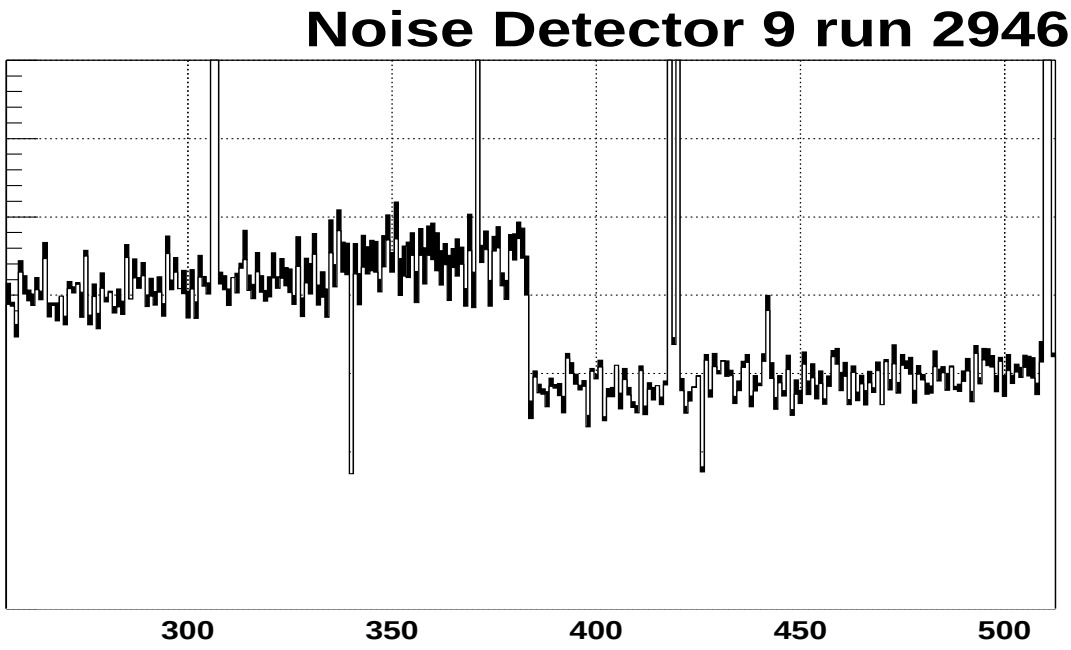

Figure 13 Noise vs. channel number for the “fast station” before (dark) and after (light) common noise suppression for a typical test-beam run.

4.3.2 Noise stability

The mean noise measured varied between different runs. In the noisy runs the mean value of the ENC increased up to 1800 e- (1300 e-) for chip 1 (chip 2). To reduce the sensitivity of the system to external influences a proper Electro-Magnetic (EM) shielding is foreseen in the next version of the FADC cards.

Figure 14 shows a comparison between a "good" run and the noisy run mentioned above for chip 2. It should be noted that the spread of the noise is greater in the good run than in the

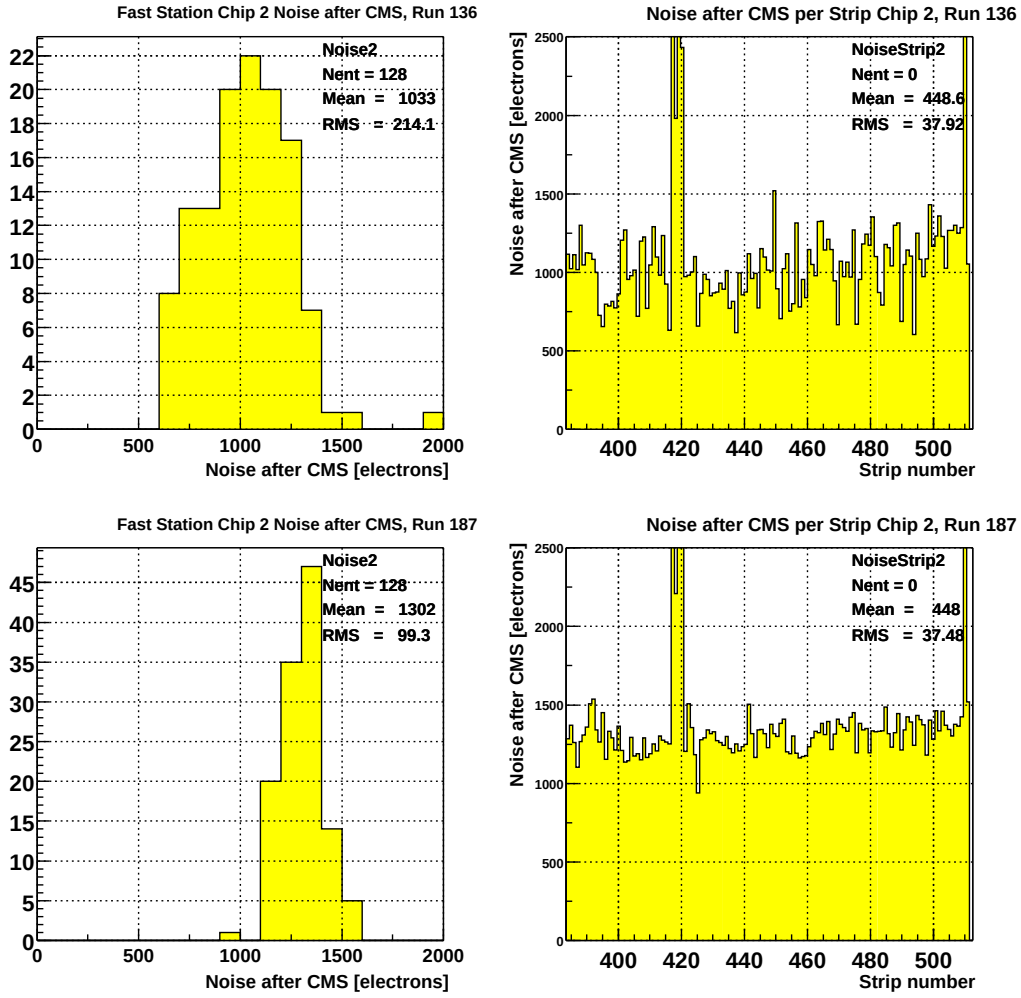

Figure 14 Noise in chip 2 for a standard (upper) and a noisy run (lower).

noisy run: this is related to the fact that 1000 e- corresponds to ~ 1 ADC count and therefore we are influenced by the ADC resolution (see section 2.2.1).

Figure 15 shows the noise in chip 1 for the same two runs as Figure 14.

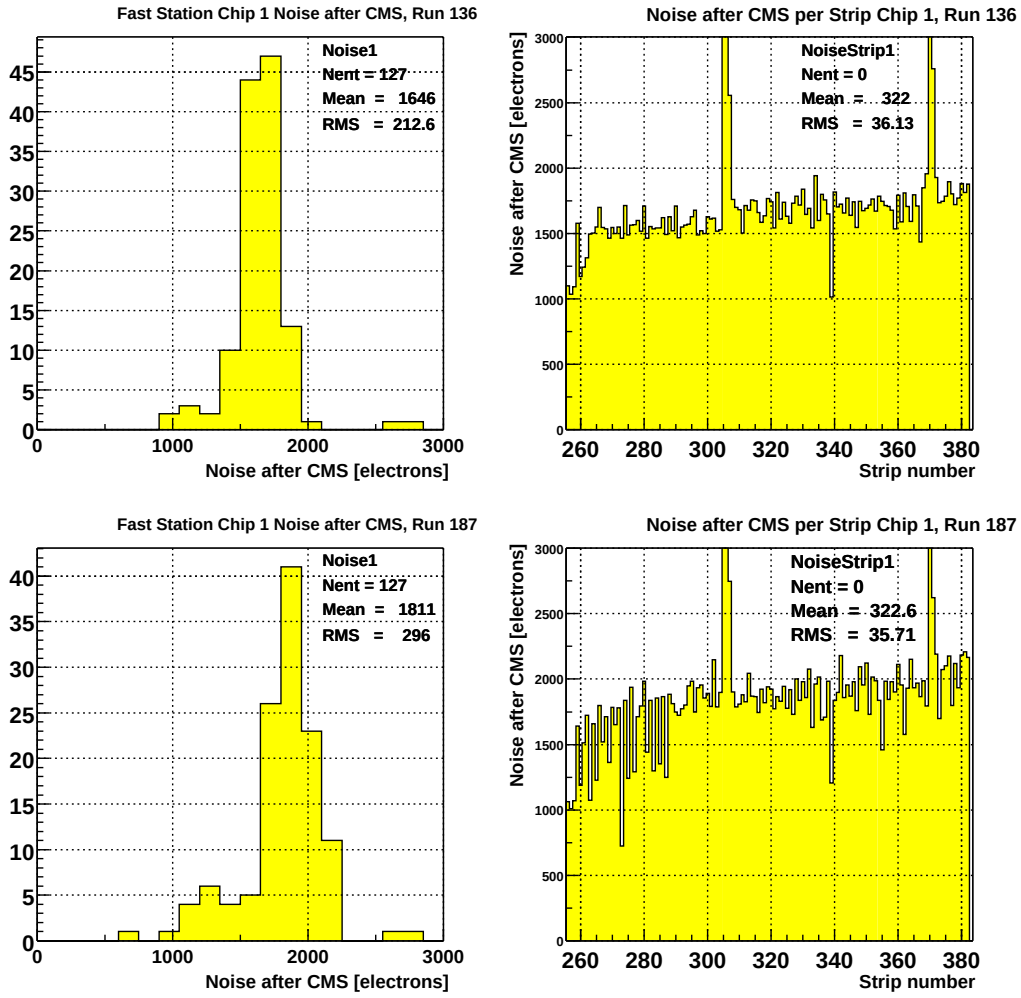

Figure 15 Noise in chip 1 for a standard (upper) and a noisy run (lower).

5 Conclusions

A test system for SCTA-128 chips and for detectors equipped with such chips has been set up. The system makes use of the prototype RB2 Digitizer for the VELO which is able to sample data at 40 MSample / s, allowing to operate the SCTA-128 chip in 40 MHz read-out mode.

The test system has been used to characterize the chips used in the summer 2000 test-beam. The chip yield was found to be ~ 40%.

We measured in the test system the noise in a PR01-R detector (also referred to as “Fast Station”): the data from test-beam allowed to calibrate the SCTA-128. We focused on two different regions of the detector, one closest to the tip and equipped with 0.6 cm - 0.8 cm long strips, the other in the external region with 3.5 cm - 4.5 cm long strips. We found qualitative and quantitative agreement with the test-beam results. The mean noise value has been found to vary in different runs: a better EM shielding in the FADC card is foreseen to reduce this effect.

Using the measured noise ranging from 1000 e- to 1300 e- for chip 1 and from 1650 e- to 1810 e- for chip 2, and the signal for one MIP measured in test-beam, we can extrapolate, for a 300 µm thick n-on-n r-type detector, a signal to noise value between 17 - 22 for the inner region and 12 - 13 for the region with strip length between 3.5 cm and 4.5 cm.

We would like to thank Raymond Frei for laboratory support and advice and Chris Parkes for support in the software setup.

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