Vertex Detector Electronics: RB3 Specification

LHCb Technical Note

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Abstract

This document is a specification of the Readout Board v.3 (RB3) for LHCB VELO and Inner Tracker detectors.

Document Status Sheet

Table 1 Document Status Sheet

1. Document Title: Vertex Detector Electronics: RB3 Specification			
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3. Issue	**4. Revision**	**5. Date**	**6. Reason for change**
Draft	0	24 Jan 2001	First version
Draft	1	6 Feb 2001	More content
Draft	2	15 Feb 2001	Added ECS interface
Draft	3	2 Mar 2001	TFC interface and Main board chapters expanded
Draft	4	30 Mar 2001	Comments from G.Haefeli on L1T preprocessor
1	0	9 May 2001	First public version

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1 Introduction

1.1 VELO electronics

The VELO (LHCb vertex detector) is located in the vacuum tank around LHCb interaction point. It is divided in 25 stations, each station has 4 silicon sensors (2K strips) attached a hybrid with 16 front-end ships. Analog signals from the hybrid are transported to repeater cards located outside of the vacuum tank and than via data links to the off-detector electronics (ODE) read-out boards located in the counting room.

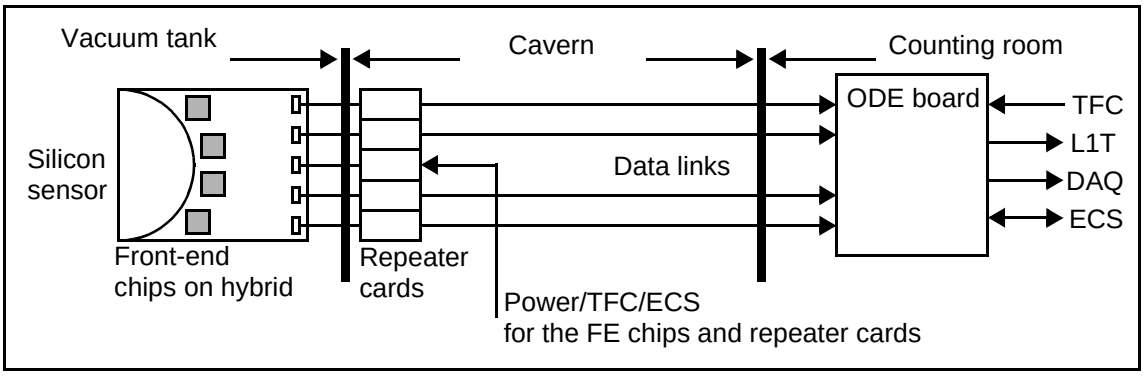

Figure 1

Power and control signals for the front-end chips are provided via separate repeater cat.

1.1.1 Front-and chip and hybrid

Two versions of the front-ens chip are now under development - SCTA_VELO (DMILL) and BEETLE (sub-micron). They both have 128 channels, 160 stages analog pipeline, 16 stages derandomiser buffer and 40 MHz analog read-out via 4 analog output links. Fast control signals are Clock, Trigger and Reset. Slow control interface is custom (similar to JTAG) for the SCTA_VELO and I2C for the BEETLE.

Hybrids carry 16 front-end chip and 5 connectors. Four connectors are allocated for the data lines and one for the power and control lines.

1.1.2 Repeater cards

There two types of the repeater cards: data and power/control. Data cards contain drivers for the data links (see 1.2). Power/control card provides connection to the analog and digital power supplies and to the timing and control systems.

1.1.3 Inner Tracker version

Inner Tracker electronics is logically the same as VELO but uses different physical implementation for the hybrids and repeater cards and different data links. The ODE read-out boards are the same as for the VELO with no trigger interface as Inner Tracker does not contribute to the trigger.

1.2 Data transmission from front-end to read-out board

The analog data from the front-end chips has to be transmitted to the read-out board (over distance of maximum 60 m for the VELO and about 100 m for the Inner Tracker) via electrical or optical analog links and converted to the digital data on the read-out board. Alternatively, analog data may be converted to the digital directly on the detector and then transmitted to the read-out board via digital optical links.

1.2.1 Twisted pair analog link (baseline for VELO)

The analog data from the front-end chip are amplified by the radiation hard link driver on the repeater card in the vicinity of the detector and transmitted to the read-out board via twisted pair analog link.

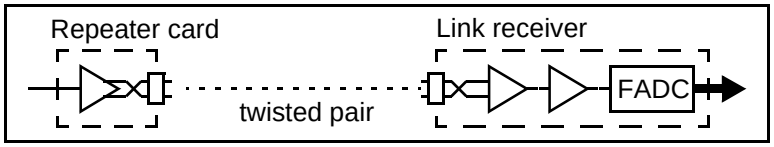

Figure 2

On the read-out board, after link receiver and amplifier, the analog signal is converted into 8-bit digit. The single link components cost estimate is given below:

Component	Comp. cost	Comp./link	Cost./link
Link driver/receiver HFA1212 / EL2142C	10.50 + 8.00 CHF	1 + 1	18.50 CHF
Connector 50-pin (32-pairs, module + cable)	8.00 + 20.00 CHF	(1/32) x 2	1.75 CHF
Screened, 18 twisted pairs, 60 m, 5 CHF/m	300.00 CHF	1/16	18.75 CHF
Amplifier AD8055	2.80 CHF	3	8.40 CHF
Dual FADC AD9059	40.00 CHF	1/2	20.00 CHF
Discrete components	10.00 CHF	1	10.00 CHF
Total			77.40 CHF

1.2.2 Digital optical link (baseline for Inner Tracker)

The analog data from the front-end chip are digitized directly on the repeater card by radiation hard FADC (Vref and clock phase control ?). Four 8-bit words are serialized and transmitted to the read-out board via 1.6 Gbit/s digital optical link (e.g. Gigabit Optical Link transmitter, GOL, from CERN microelectronics group). Parallel optical transmitter and receiver (VCSEL) and ribbon fible cable may be used to transfer the data.

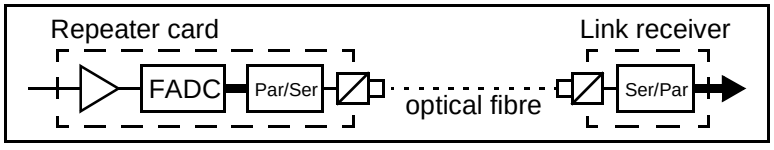

Figure 3

Parallel optical link receiver perform optical to electrical conversion. The ncoming data are deserialized. The single link components cost estimate is given below:

Component	Comp. cost	Comp./link	Cost./link
Radiation hard 12-bit FADC AD9042	25.00 CHF	1	25.00 CHF
GOL Serializer (32->1)	20.00 CHF	1/4	5.00 CHF
Optical transmitter (12 VCSEL)	900.00 CHF	1/48	18.75 CHF
Connectorized optical fibres, 100 m	1300.00 CHF	1/48	27.00 CHF
Optical receiver (12 VCSEL)	900.00 CHF	1/48	18.75 CHF
Deserializer TLK2500 (16->1) and demux	80.00 CHF	1/4	20.00 CHF
Discrete components	5.00 CHF	1	5.00 CHF
Total			120.00 CHF

1.3 Read-out board

1.3.1 General description

Read-out Board version 3 (RB3) is a 16-input prototype of a final 64-input read-out board for the LHCb vertex and inner tracker detectors. The board receives multiplexed signals from the vertex detector (or inner tracker) front-end chips via data transmission links. The board is composed of 4 identical data channels, each processing data from four input links. Data channel contains link receiver (1), synchronisation logic (2), preprocessor for the level-1 trigger (3), level-1 buffer (4) and data processor for the DAQ system (5).

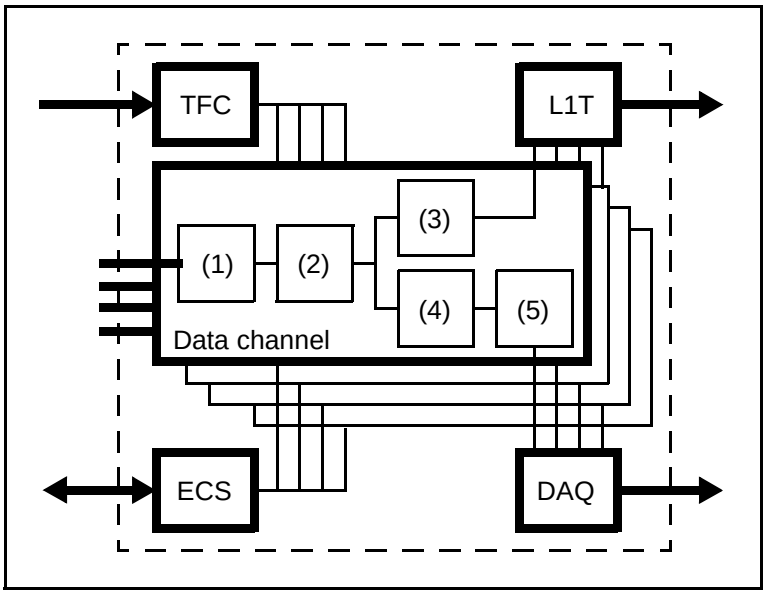

Figure 4

Four interfaces to the external systems - timing and fast control (TFC), level-1 trigger (L1T), data acquisition (DAQ) and experiment control (ECS) systems are common for all data channels and designed in such a way that may be used also for 16 data channels on the final 64-input read-out board. Some features of the RB3 may not be implemented on the final version if found unnecessary. On the inner tracker version of the board the preprocessor for the level-1 trigger (4) and the level-1 trigger (L1T) interface are not installed. The link receivers (1) may be also different.

1.3.2 Implementation

The board is implemented as a 9U module (366.70 mm x 400.00 mm, IEEE1101.10 mechanics) and occupies two slots in the crate. LHCb custom power distribution backplane in J3 position in the crate provides the power to the boards, VME backplane is not used. Alternatively, standard 9U VME crate may be used (VME connector provides only power to the board).

The board uses standard commercial (non radiation hard or radiation tolerant) components. Some functional parts of the board (e.g. link receiver, level-1 buffer, etc.) are implemented on daughter cards for possible different implementation without modification of the main RB3 board.

2 Data channel functional blocks

2.1 Link receiver for analog links

This functional block consists of 4-channels FADC card and timing and control logic on the main board.

2.1.1 FADC daughter card

FADC card (twisted pair version) contains line receivers (1), line equalizers (2), amplifiers (3), and analog-to-digital converters (4). The main parameters of the 4-channels FADC card are:

- Inputs: four 2-pin LEMO302 connectors, differential, 0 to 1 Volt range,
- FADC: Analog Devices AD9059 / AD9057 [1] (8-bit, 60 MSPS), adjustable Vref and clock phase,
- FADC pipeline delay: 3 clock cycles (? +1), FADC output propagation delay: 9.5 ns (max 14.2 ns),
- Power: +5V digital (? mA), +5V analog (? mA), -5V analog (? mA),
- Main board connectors, ERNI063.653: 50-pin connector for digital and 12-pin connector for analog,
- Dimensions: 117 mm x 71 mm.

Layout of 50-pin connector for digital signals is shown below:

Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
GND_DIGITAL	1	2	GND_DIGITAL	FADC_2(4)	27	28	FADC_2(5)
FADC_0(0)	3	4	FADC_0(1)	FADC_2(6)	29	30	FADC_2(7)
FADC_0(2)	5	6	FADC_0(3)	GND_DIGITAL	31	32	GND_DIGITAL
FADC_0(4)	7	8	FADC_0(5)	FADC_3(0)	33	34	FADC_3(1)
FADC_0(6)	9	10	FADC_0(7)	FADC_3(2)	35	36	FADC_3(3)
GND_DIGITAL	11	12	GND_DIGITAL	FADC_3(4)	37	38	FADC_3(5)
FADC_1(0)	13	14	FADC_1(1)	FADC_3(6)	39	40	FADC_3(7)
FADC_1(2)	15	16	FADC_1(3)	GND_DIGITAL	41	42	GND_DIGITAL
FADC_1(4)	17	18	FADC_1(5)	CLOCK_0	43	44	CLOCK_1
FADC_1(6)	19	20	FADC_1(7)	CLOCK_2	45	46	CLOCK_3
GND_DIGITAL	21	22	GND_DIGITAL	GND_DIGITAL	47	48	GND_DIGITAL
FADC_2(0)	23	24	FADC_2(1)	+5V_DIGITAL	49	50	+5V_DIGITAL
FADC_2(2)	25	26	FADC_2(3)				

Layout of 12-pin connector for analog signals is shown below:

Signal	Pin	Pin	Signal
+5V_ANALOG	1	2	+5V_ANALOG
GND_ANALOG	3	4	GND_ANALOG
-5V_ANALOG	5	6	-5V_ANALOG
VREF_0	7	8	VREF_1
VREF_2	9	10	VREF_3
GND_ANALOG	11	12	GND_ANALOG

FADC card dimensions and connector positions are shown below (view from the component side):

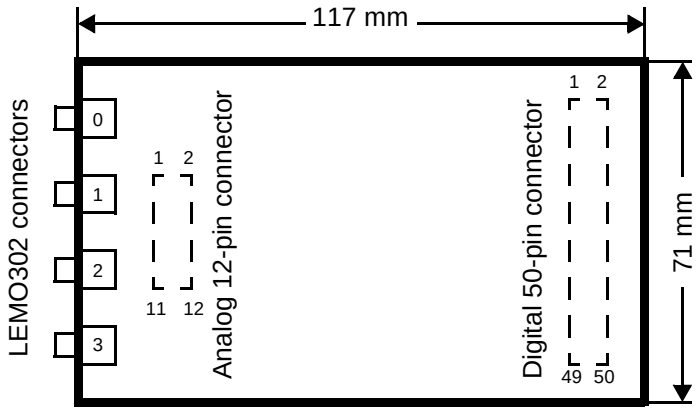

Figure 5

2.1.2 Timing and control logic on the main board

For each FADC card the main board provides 4 individually controlled Vref voltage and clock signals in order to allow individual control per input link. This is possible in a case of using AD9057 single channel FADC, for the dual FADC version (AD9059) Vref and clock are controlled per pair of input links.

Analog power supply voltage for the FADC card are supplied by the custom power distribution backplane or generated from +12V and -12V on VME connector using power regulators, located on the main board.

2.1.2.1 FADC card reference voltage

Adjustable reference voltage for the FADC card is provided by the Mitsubishi M62399P [2] octal 8-bit DAC with 5 ms setup time, I2C read/write control interface and Reset input. Up to 8 such devices may be connected to one I2C bus (from ECS controller) using 3 chip select pins (A2..A0), each device uses one I2C address. I2C bus data format is shown below:

START	SLAVE ADDRESS	W	A	SUB ADDRESS	A	DAC DATA	A	STOP

- SLAVE ADDRESS: [1, 0, 0, 1, A2, A1, A0], where [A2..A0] - chip select
- SUB ADDRESS: [X, X, X, X, S3, S2, S1, S0], where [S3..S0] - channel select

One DAC provides 8 adjustable reference voltage, selected by channel select bits (S3..S0) and may be used for two FADC cards on RB3 board. In total, there are 2 devices on the board, they use 2 I2C addresses and provide 16 reference voltage. Setup time for one channel is 29 I2C clock cycles.

Alternative device is MAXIM MAX521 [3] octal 8-bit DAC with 6 ms setup time and I2C write only control interface (written DAC settings can't be read back).

> *For the final ODE board only one reference voltage per FADC card may be needed, 16 in total. Therefore, the same 2 devices may be used for the final 64-channel board.*

2.1.2.2 FADC card clock

FADC card clock is generated from the main board clock, delivered by the TFC system, using TTCrx receiver chip (see 3.1.1). The main board clock may be delayed inside the TTCrx chip with 104 ps step (relatively to the incoming TFC clock. This allow a board wide clock phase adjustment relatively to the incoming analog data.

Individual clock phase adjustment with 1 ns step is performed using 4-channels PHOS4 [4] delay chip. Each channel can be programmed via I2C write only control interface. Up to 16 such devices may be connected to one I2C bus (from ECS controller) using 4 chip select pins (A5..A2), each device uses four I2C addresses. I2C bus data format is shown below:

START	SLAVE ADDRESS	0	A	CHANNEL DATA	A	STOP

- SLAVE ADDRESS: [0, A5, A4, A3, A2, X, X], where [A5..A2] - chip select
- CHANNEL DATA: [S2, S1, S0, D4, D3, D2, D1, D0], where [S2..S0] - channel select, [D4..D0] - data

The PHOS4 chip has no reset signal. The first negative transition on the I2C clock line after power-up is used to trigger the reset procedure. Therefore the first data transmission to the PHOS4 chip will have no any effect on the delay registers.Clock input has to be active during the reset.

One PHOS4 chip is used for one FADC card on RB3 board. In total, there are 4 devices on the board, they use 16 I2C addresses and provide 16 clocks. Setup time for one channel is 20 I2C clock cycles.

For the final ODE board only one adjustable clock per FADC card may be needed, 16 in total. Therefore, the same 4 devices may be used for the final 64-channel board.

2.2 Link receiver for digital link

TBD

2.3 Synchronization logic

Synchronisation logic (SyncFPGA) in the data channel processes the data coming from one front-end chip over 4 input links and digitized in one FADC card (DATA_FADC). The event data format over 4 input links from the (Beetle) chip is the following: first two samples on 4 links carry distributed HEADER(7..0) - 8-bit front-end chip pipeline column number or PCN (binary data coded as analog levels or pseudo-digital bits) following by 128 analog samples of detector data (32 samples per link) from front-end chip analog inputs connected to the detector channels:

Link_3	Link_2	Link_1	Link_0
HEADER(7)	HEADER(5)	HEADER(3)	HEADER(1)
HEADER(6)	HEADER(4)	HEADER(2)	HEADER(0)
ANALOG_IN(127)	ANALOG_IN(95)	ANALOG_IN(63)	ANALOG_IN(31)
...	...	...	...
ANALOG_IN(96)	ANALOG_IN(64)	ANALOG_IN(32)	ANALOG_IN(0)

SyncFPGA performs the following tasks:

- synchronisation of the FADC output data to the internal SyncFPGA logic (1), synchronisation error check (using data from TFC and neighbouring SyncFPGAs) and error monitoring (2),
- data formatting for the level-1 trigger preprocessor and the level-1 buffer (3),
- interfacing to the ECS controller via read / write control interface (4) for parameter setting and monitoring and write access to the level-1 buffer for test purposes.

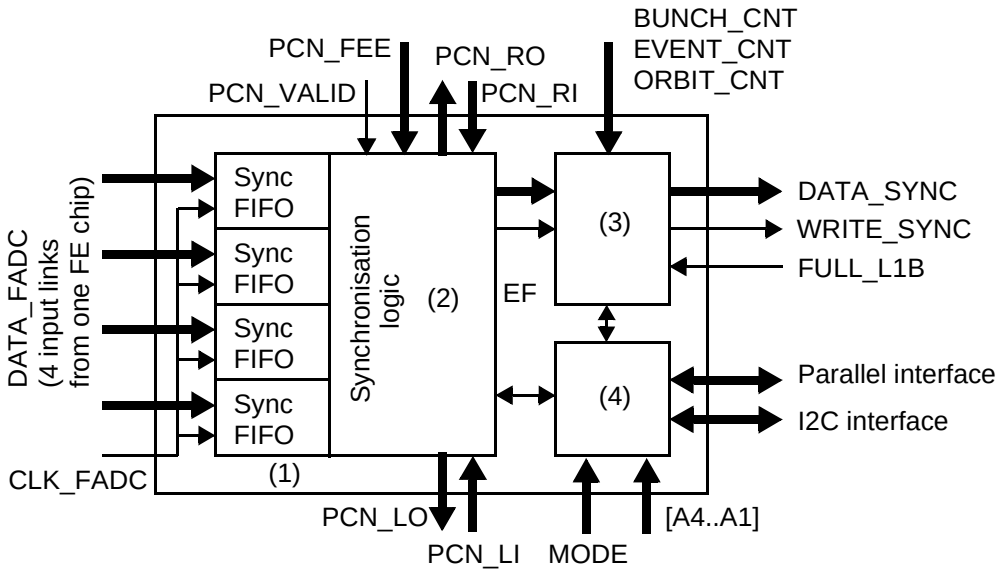

Figure 6

SyncFPGA operation mode is defined by signals on MODE pins which are connected to the timing / control FPGA in the TFC interface. The SyncFPGA address for the I2C interface is defined by pins (A4..A1).

In the final 64-input read-out board there are 16 SyncFPGAs, therefore 4 chip select pins (A4..A1) are necessary.

2.3.1 Input data synchronisation

FADC card clock may has different phase relatively to the SyncFPGA clock. In order to synchronise FADC output data to the SyncFPGA clock an input synchronisation FIFO may be used. It uses FADC card clock as FIFO write clock and SyncFPGA clock as FIFO read clock. The data are constantly written to the FIFO and read out. (This FIFO may add an extra pipeline delay to the FADC data path - one or two clocks, depending on the FADC clock delay, set in the PHOS4 chip (?)).

The input FIFO is also may be used as a test memory (128 words). The test mode is defined by the SyncFPGA control pins (MODE). In this mode data are written to the FIFO from the ECS controller and may be read back. Data from the FIFO are used to test the RB3 operation.

If the input synchronisation FIFO is not implemented some restriction shall be set on the possible clock phase adjustment range in the PHOS4 delay chip for the FADC card.

2.3.2 Synchronisation check

In the synchronisation logic, 8-bit FADC data from 4 input links are converted into 4 pseudo-digital bits. Two I2C registers hold the limits for high and low thresholds, used to convert 8-bit data into the pseudo-digital bit. The 8 pseudo-digital bits from two consecutive samples (PCN from the front-end chip) are compared with the 8-bit PCN_FEE value, generated by the timing/control FPGA in the TFC interface, during “PCN_VALID” signal. The error flag EF_T is set, if these values are different.

In order to perform inter-SyncFPGA’s cross-check, the value of the PCN from the front-end chip is also sent to the right and left neighbouring SyncFPGAs (as PCN_RO and PCN_LO) and compared with the PCN value generated in the right and left neighbouring SyncFPGAs (as PCN_RI and PCN_LI) and error flags EF_R and EF_L are set, if these values are different.

Error flags are sent together with event data to the level-1 trigger preprocessor and to the level-1 buffer. They are also counted by three (8-bit ?) counters, accessible via control interface for read and reset.

2.3.3 Interface to level-1 trigger preprocessor and L1B

This block writes event data from 4 input data links into the level-1 trigger preprocessor and to the level-1 buffer as 32-bit wide data (DATA_SYNC). Data format is similar to the input data format (DATA_FADC) with the original distributed HEADER (pseudo-digital PCN) substituted by event identification, generated by TFC system (8-bit PCN, 8-bit ORBIT_CNT, 12-bit BUNCH_CNT, 24-bit EVENT_CNT) and error flags (check with the Level-1 Trigger and DAQ Read-out Unit data formats).

DATA_SYNC(31..24)	DATA_SYNC(23..16)	DATA_SYNC(15..8)	DATA_SYNC(7..0)
00000, EF_L, EF_R, EF_T	EVENT_CNT(23..16)	EVENT_CNT(15..8)	EVENT_CNT(7..0)
ORBIT_CNT(7..0)	0000, BUNCH_CNT(11..8)	BUNCH_CNT(7..0)	PCN(7..0)
ANALOG_IN(127)	ANALOG_IN(95)	ANALOG_IN(63)	ANALOG_IN(31)
...	...	...	...
ANALOG_IN(96)	ANALOG_IN(64)	ANALOG_IN(32)	ANALOG_IN(0)

Some ANALOG-IN data re-ordering may be necessary in a case where detector channels are not connected to the front-end chip analog inputs in spacial order (inside the group of 32 channels) for the preprocessing. Full signal from the Level-1 buffer (FULL_L1B) may be used in some specific modes of operation and ignored during standard data taking mode.

2.3.4 TFC interface

From the TFC interface, SyncFGA receives the following information:

- 8-bit pipeline column number (PCN_FEE), generated by the front-end emulator in the TFC interface, accompanied by the PCN_VALID flag,
- event identification information: 12-bit bunch crossing counter (BUNCH_CNT), 8-bit orbit counter (ORBIT_CNT), 24-bit event counter (EVENT_CNT),
- two MODE<1..0> bits define the operation mode of the SyncFPGA.

2.3.5 Control interface

Several 8-bit internal registers in the SyncFPGA have to be accessible from the ECS controller on the main RB3 board, namely:

- 4 registers to write / read data to / from 4 input synchronisation FIFOs,
- 2 registers to hold the limits for high and low thresholds for the pseudo-digital bit conversion,
- 3 synchronisation error counters for EF_T, EF_R and EF_L,
- 1 data register for DATA_SYNC output to write data into level-1 buffer for test purposes.

These eight internal SyncFPGA registers are accessible via two read / write control registers in SyncFPGA control interface - address and data registers. The address register holds the address of the internal SyncFPGA register. Writing to the data register means writing into the internal SyncFPGA register, selected by the contents of the address register. Reading from the data register means reading from the internal SyncFPGA register, selected by the contents of the address register.

Access to these two control registers is possible via two external interfaces - parallel and I2C, implemented for the evaluation purposes in order to choose the final one.

2.3.5.1 Parallel interface

Parallel interface is simpler to implement and faster but requires more pins on the SyncFPGA. The minimum set of signals to implement 8-bit parallel interface is shown below:

- DATA_ECS - 8-bit data path to write and read the data to / from the control registers,
- WR - write signal, defines the direction of the data transfer on the data path,
- AD - address bit to select control register (AD=0 - address register, AD=1 - data register),
- CS - chip select to select SyncFPGA by the ECS interface on the main RB3 board.

The CS signal is generated in the ECS controller on the main RB3 board (by address decoder) in order to avoid many parallel address lines to the SyncFPGAs.

2.3.5.2 I2C interface

I2C interface needs less pins on the SyncFPGA but slower and more complicated than parallel interface. Address and data control registers may be accessed separately or in a single address / data I2C transaction.Block transfer to the data register is possible (e.g. to write / read the input synchronisation FIFOs). I2C bus data format for the latter case is shown below (write to the internal SyncFPGA register, selected by the [S2..S0] bits in the address register):

START	SLAVE ADDRESS	W	A	REG ADDRESS	A	REGISTER DATA	A	STOP

- SLAVE ADDRESS: [0, 0, A4, A3, A2, A1, AD], where [A4..A1] - chip select, AD=0 (address)
- REG ADDRESS: [X, X, X, X, X, S2, S1, S0], where [S2..S0] - internal register select

2.3.6 SyncFPGA pin count and possible device

Signal	N pins	in/out	Int FPGA Src/Dst	Ext Blk
DATA_FADC,	32+4	in	Synchronisation	FADC card
CLK_FADC	4	in	Synchronisation	PHO4 chip
BUNCH_CNT, EVENT_CNT, ORBIT_CNT	12+24+8	in	Synchronisation	TFC
PCN_FEE, PCN_VALID	8+1	in	Synchronisation	TFC
PCN_RO, PCN_LO, PCN_RI, PCN_LI	8+8+8+8	out	Synchronisation	SyncFPGA
DATA_SYNC, WRITE_SYNC, FULL_L1B	32+1+1	out	L1T/L1B interface	L1T/L1B
Reserved	2	-	L1T/L1B interface	L1T/L1B
SDA, SCL (I2C interface)	1+1	inout+in	Control interface	ECS
[A4..A1] (I2C chip select)	4	in	Control interface	h/w pins
DATA_ECS, AD, CS, WR	8+3	inout	Control interface	ECS
MODE	2	in	Internal logic	TFC
CLK_MAIN, RST	2	in	Internal logic	TFC
Total	172			

Altera APEX 20K100/100E, 240-pin package, 189/181 user pins (?).

2.3.7 SyncFPGA configuration

All SyncFPGAs on the RB3 board may be configured in parallel from a Flash EEPROM(s) (e.g. EPC2 or EPC4 for Altera devices, to be studied) via FPGA configuration port (1). An “EEPROM pool” of several EEPROMs may be used to configure several different types of FPGAs used on the RB3 board (see ECS interface chapter). Configuration is also possible via download cable using a connector on the RB3 board. Optionally, FPGA configuration may be performed from the ECS controller memory via FPGA JTAG port (2). The EPROM can be re-programmed from the ECS controller memory via EPROM JTAG port (3). This feature allows in-cite FPGA upgrade and requires software support in the ECS controller.

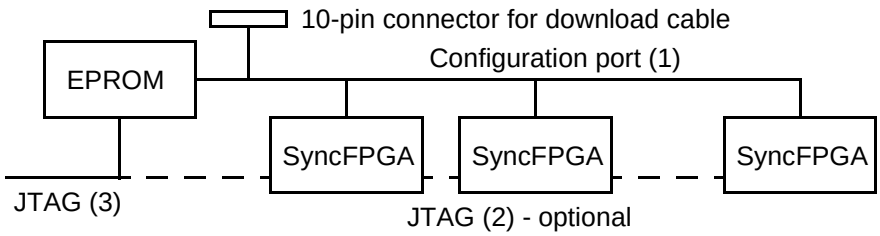

Figure 7

2.4 Level-1 trigger preprocessor

Level-1 trigger preprocessing FPGA (PpFPGA) in the data channel processes the data coming from two SyncFPGAs (DATA_SYNC) - 8 input links or 256 detector channels. PpFPGA performs the following tasks:

- data processing (pedestal subtraction, fulty channel masking, common mode suppression, hit detection and reordering) in processing blocks,
- cluster encoding, collectin and transferring them to the Level-1 trigger interface (LinkFPGA),
- interfacing to the ECS controller for parameter setting and monitoring via read/write control interface.

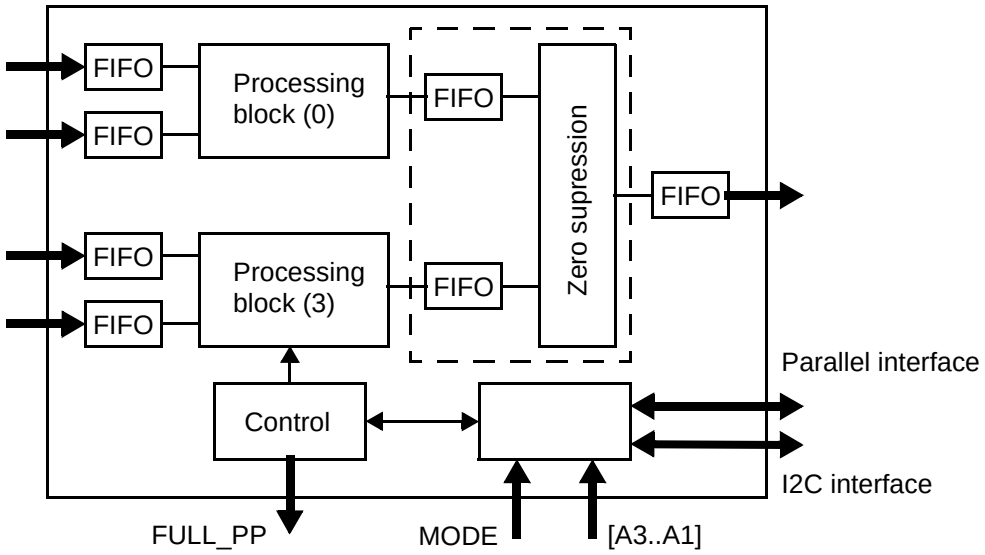

Figure 8

PpFPGA operation mode is defined by signals on MODE pins which are connected to the timing/control FPGA in the TFC interface. The SyncFPGA address for the I2C interface is defined by pins (A3..A1).

In the final 64-input read-out board there are 8 PpFPGAs, therefore 3chip select pins (A3..A1) are necessary.

2.4.1 Processing block

Each processing block has 2 input FIFOs, algorithm block and output FIFO. The input FIFOs receives the data DATA_SYNC from the SyncFPGA (see 2.3.3). The algorithm block performs pedestal subtraction and common mode suppression. It works at double frequency and processes the data from two input FIFOs in sequence. Detected hits are stored in the 64-word deep FIFO. Each preprocessing channel has two 32*8 RAM blocks for pedestals and hit thresholds.

2.4.2 Zero supression

For each event, hits from FIFOs are encoded, collected, counted and stored as 9-bit addresses (5-bit hit address, 1 bit cluster suze, 3-bit preprocessing channel number) in the 128-word deep output FIFO. After that,

they are transferred to the LinkFPGA in the level-1 trigger (L1T) interface. Data format is shown below:

DATA_PpFPGA(8..0)
EVENT_CNT(4..0), Overflow, EF_L, EF_R, EF_T
000, Number_of_clusters(5..0)
Cluster_Address_0
...
Cluster_Address_N

Mapping of the Hit_Address to the detector channel number shall be provided in due course.

2.4.3 Control interface

Several 8/16-bit internal registers and dedicated RAMs in the PpFPGA have to be accessible from the ECS controller on the main RB3 board, namely:

- 8 (one per processing channel) pedestal LUTs (32*8),
- 8 (one per processing channel) hit threshold LUTs (32*8),
- 8 (one per processing channel) 32-bit channel mask registers,
- 4 processing monitoring registers, algorithm parameters.

These internal PpFPGA registers are accessible via two read/write control registers in PpFPGA control interface - address and data registers. The address register holds the address of the internal PpFPGA register. Writing to the data register means writing into the internal PpFPGA register, selected by the contents of the address register. Reading from the data register means reading from the internal PpFPGA register, selected by the contents of the address register.

Access to these two control registers is possible via two external interfaces - parallel and I2C, implemented for the evaluation purposes in order to choose the final one.

2.4.3.1 Parallel interface

Parallel interface is simpler to implement and faster. The minimum set of signals to implement 16-bit parallel interface is shown below:

- DATA_ECS - 16-bit data path to write and read the data to/from the control registers,
- WR - write signal, defines the direction of the data transfer on the data path,
- AD - address bit to select control register (AD=0 - address register, AD=1 - data register),
- CS - chip select to select PpFPGA by the ECS interface on the main RB3 board.

The CS signal is generated in the ECS controller on the main RB3 board (by address decoder) in order to avoid many parallel address lines to the PpFPGAs.

2.4.3.2 I2C interface

I2C interface needs less pins on the PpFPGA but is slower and is more complicated than parallel interface. Address and data control registers may be accessed separately or in a single address/data I2C transaction. I2C bus data format for the latter case is shown below (write to the internal PpFPGA register, selected by the

[S2..S0] bits in the address register):

START	SLAVE ADDRESS	W	A	REG ADDRESS	A	REGISTER DATA	A	STOP

- SLAVE ADDRESS: [0, 0, 0, A3, A2, A1, AD], where [A3..A1] - chip select, AD=0 (address)
- REG ADDRESS: [X, X, X, X, X, S2, S1, S0], where [S2..S0] - internal register select

Block transfer to the data register is possible (e.g. to write / read LUTs).

2.4.4 PpFPGA pin count and possible device

Signal	N pins	in/out	Int FPGA Src/Dst	Ext Blk
DATA_SYNC	32+32	in	Preprocessing channel	SyncFPGA
WRITE_SYNC	1+1	in	Preprocessing channel	SyncFPGA
DATA_PREP	9	out	Read-out Block	LinkFPGA
WRITE_PREP	1	out	Read-out Block	LinkFPGA
FULL_RO	1	out	Read-out Block	TFC
FULL_PP	8	out	Control Block	TFC
SDA, SCL (I2C interface)	1+1	inout+in	Control interface	ECS
[A3..A1] (I2C chip select)	3	in	Control interface	h / w pins
DATA_ECS, AD, CS, WR	16+3	inout	Control interface	ECS
MODE	2	in	Internal logic	TFC
CLK_MAIN, RST	2	in	Internal logic	TFC
Total	104			

Altera APEX 200E, 240-pin package, 189 / 181 user pins (?).

2.4.5 PpFPGA configuration

Configuration of the PpFPGA is similar to the SyncFPGA (see 2.3.7).

2.5 Level-1 trigger interface

Level-1 trigger (L1T) interface is implemented in one FPGA (LinkFPGA) and performs the following tasks:

- read-out the event fragments from 8 PpFPGAs,
- encapsulets the data according to the S-Link requirements,

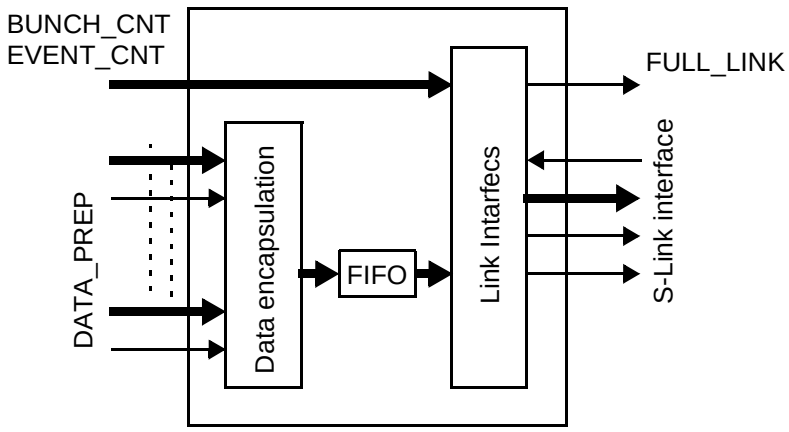

Figure 9

2.5.1 Data Encapsulation

Data read from the PpFPGAs are collected, formatted and written into 256-word deep FIFO in the Link Interface. Data format is described in the following chapter.

2.5.2 Link Interface

Link Interface sends the formatted data to the Level-1 Trigger via data link. The interface to the trigger link is defined as 32-bit S-Link [6] without specifying the physical implementation of the S-Link.

2.5.2.1 S-Link

The S-Link interface is a simple FIFO-like interface. The S-Link interface specification describes the interface (connector and protocol) between the Front-end Motherboard (FEMB, in our case - RB3 board) and the Link Source Card (LSC) and the interface between the Link Destination Card (LDC) and the Read-out Motherboard (ROMB, in out case - Read-out Unit of the DAQ system). It does not describe the physical link itself. A maximum clock frequency for the S-Link interface is defined as 40 MHz (the data transfer rate on the physical link may be differ). All word transmitted by the S-Link are accompanied by a control / data bit. A data block is defined as the data words between two control words.

A return channel exists which allows the LDC to pass information back to the LSC. The main function of this return channel is to transmit flow control commands from the Read-out Unit to the RB3. Thus the S-Link transmits only when the Read-out Unit is available to read the data. When the Read-out Unit is unavailable, data transfers from the RB3 to the S-Link are inhibited.

Recommended S-Link physical link card layout is based on single side Common Mezzanine Card standard. The card size is 149 x 74 mm^2. Single 64-pin connector is used for signals and power. The connector layout (viewed onto the RB3 board) is shown below:

Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
LRL3	1	2	LRL2	UD23	33	34	UD22
Vcc	3	4	LRL1	UD21	35	36	GND
Vcc	5	6	LRL0	UD20	37	38	UD19
LDOWN#	7	8	GND	Vcc	39	40	UD18
GND	9	10	LFF#	UD17	41	42	UD16
UCLK	11	12	GND	UD15	43	44	GND
GND	13	14	UWEN#	UD14	45	46	UD13
URESET#	15	16	GND	GND	47	48	UD12
UDW1	17	18	UTEST#	UD11	49	50	UD10
UCTRL#	19	20	UDW0	UD9	51	52	Vcc
UD31	21	22	Vcc	UD8	53	54	UD7
GND	23	24	UD30	GND	55	56	UD6
UD29	25	26	UD28	UD5	57	68	UD4
UD27	27	28	GND	UD3	59	60	GND
UD26	29	30	UD25	UD2	61	62	UD1
GND	31	32	UD24	Vcc	63	64	UD0

2.5.2.2 Data format

Data format for the Level-1 Trigger event data consists of S-Link transport data format [6], proposed by the Readout Unit, which contains the VELO detector data itself, in the format, proposed in the Levl-1 Trigger requirements document [7].

The S-Link transport data format consists of 3 header words and one or two trailers as shown below. The first and the last words in the data format are S-Link control words, accompanied by a control bit.

UD(31..0)	UCTRL#
0000, EVENT_CNT(23..0), 0000	'0'
LINK_ID(15..0), CHECK_BITS(7..0), TYPE(7..0)	'1'
ERROR_BLOCK_OFFSET(15..0), RESERVED(7..0), ERROR_BLOCK_SIZE(7..0)	'1'
DATA_BLOCK(31..0)	'1'
...	'1'
ERROR_BLOCK(31..0) - optional	'1'
STATUS(7..0), TOTAL_SIZE(19..0), 0000	'0'

The meanings of different fields are:

- EVENT_CNT - 24-bit event counter from TFC system interface,
- LINK_ID - 16-bit link identifier (link number), set by the ECS,
- CHECK_BITS - (optional, TBD) 8-bit check bits field, default is zero,
- TYPE - (optional, TBD) 8-bit field for type of data, default is zero,

- ERROR_BLOCK_OFFSET - 16-bit offset to the optional error block, ignored, if SIZE_EB is zero (in fact, this is a DATA_BLOCK_SIZE),
- ERROR_BLOCK_SIZE - 8-bit size of ERROR_BLOCK (number of 32-bit words in ERROR_BLOCK)
- DATA_BLOCK - VELO detector data, N x 32-bit data words,
- ERROR_BLOCK - (optional, TBD) description of error history in the Readout Unit, default is zero,
- STATUS - (TBD) 8-bit of fast status information for 8 error classes, default is zero,
- TOTAL_SIZE - 20-bit total number of 32-bit words in the event data (4+DBS+EBS).

The 16-bit standard VELO detector data format, proposed in [7], consists of two header words, sub-header word and data words It may be packed into 32-bit wide DATA_BLOCK of the S-Link transport data format, described above.

DATA(15..0)
FMT(1..0), STATION_NUMBER(5..0), TOTAL_WORD_COUNT(7..0)
ORBIT_CNT(3..0), BUNCH_CNT(11..0)
SECTOR_NUMBER(2..0), 0, HIT_CNT_N(5..0), HIT_CNT_M(5..0)
DATA_WORD_0
...
DATA_WORD_N

The meanings of different fields are:

- FMT - 2-bit event format (‘0’ - reserved, ‘1’ - standard format, ‘2’ - synchronisation format),
- STATION_NUMBER - 6-bit station identifier (5 bits of LINK_ID in S-Link transport data format ?),
- TOTAL_WORD_COUNT - 8-bit total number of 16-bit words including headers and sub-header (DATA_BLOCK_SIZE / 2 in the transport data format ?),
- ORBIT_CNT - 4 least significant bits of the 8-bit orbit counter in TFC system interface,
- BUNCH_CNT - 12-bit bunch counter in the TFC system interface,
- SECTOR_NUMBER(2..0) - 2-bit sector identifier in the station (a sensor identifier ?),
- HIT_CNT_N, HIT_CNT_M - 6-bit hit counts (TBD),
- DATA_WORD_N - 14-bit hit coordinate (11-bit for 2K strips on the sensor?), 1-bit C (‘0’ - left, ‘1’ - right), 1-bit L (‘0’ - single hit cluster, ‘1’ - multi hit cluster) - TBD.

The synchronisation event (FMT=2), as proposed in [7], is generated on each increment of the orbit counter (every 89 μs). - TBD, do we need it ?

Alternative 16-bit data format is also described in [8]. It proposes a possible cluster encoding scheme with maximum cluster size of two hits, bigger clusters are encoded as several small clusters.

A proposed 32-bit data format for the VELO ODE to be sent to the L1T is the following:

DATA(15..0)
Mode, Sensor_number(6..0), Number_of_clusters(7..0), Flags(3..0), Bunch_counter(11..0)
Cluste_address_0(11..0)
...
Cluste_address_N(11..0)

2.5.2.3 S-Link physical implementation

Several physical implementations of the S-Link exist, ranging from parallel electrical (differential or LVDS) to serial optical links. The the Link Source Card on the RB3 board must be compatible with the Link Destination Card in the Readout Unit. The electrical S-Link may be suitable because the read-out boards and the level-1 trigger electronics will be both located in the counting room.

2.5.3 TFC interface

The output FIFO in the Link Interface block may overflow. The full flag may be sent out of LinkFPGA for further processing in TFC interface.

Two MODE<1..0> bits define the operation mode of the LinkFPGA.

2.5.4 Control interface

The following parameters have to be loaded into the LinkFPGA:

- LINK_ID - 16-bit link identifier (link number)

They are accessible via LinkFPGA control interface.

2.5.5 LinkFPGA pin count and possible device

Signal	N pins	in/out	Int FPGA Src/Dst	Ext Blk
DATA_EVENT	72	in	Synchronisation	
WRITE_EVENT	8	in	L1T preprocessor interface	
BUNCH_CNT, EVENT_CNT	12+24	in	Synchronisation	TFC
UD[31..0]	32	out	Data formatting	S-Link LDC
S-Link ccontrol signals	5	in / out	Data formatting	S-Link LDC
FULL_LINK	1	out	Data formatting	TFC
SDA, SCL (I2C interface)	1+1	inout+in	Control interface	ECS
[A3..A1] (I2C chip select)	3	in	Control interface	h / w pins
DATA_ECS, AD, CS, WR	16+3	inout	Control interface	ECS
MODE	2	in	Internal logic	TFC
CLK_MAIN, RST	2	in	Internal logic	TFC
Total	170			

Altera APEX 20K100 / 100E, 240-pin package, 189 / 181 user pins (?).

2.5.6 LinkFPGA configuration

Configuration of the LinkFPGA is similar to the SyncFPGA (see 2.3.7).

2.6 Level-1 buffer, data processor and DAQ interface

Level-1 buffer, data preprocessor and DAQ interface on the RB3 are implemented as a daughter card (DAQI card, a single card per RB3 board). The final implementation of this functional part of the read-out board will be chosen after testing prototypes on the RB3 board.

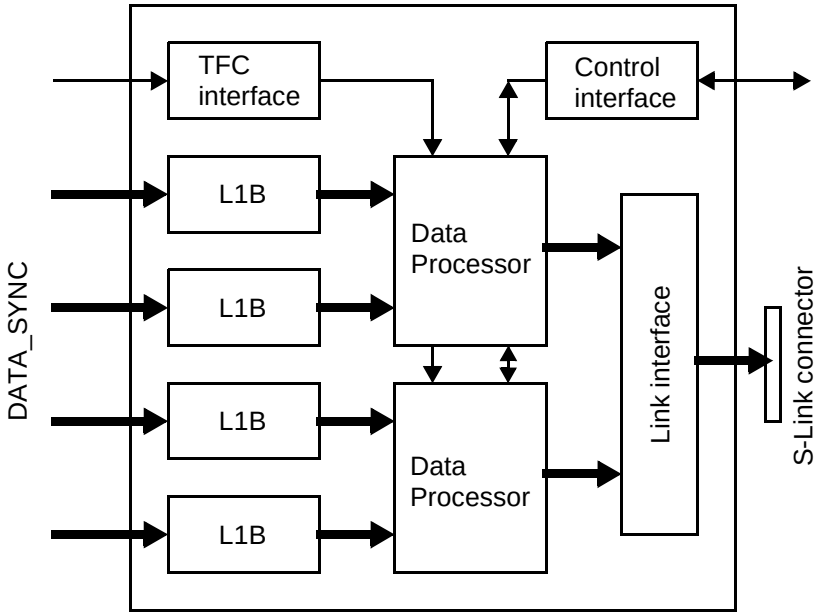

Figure 10

It receives the data from four SyncFPGAs (DATA_SYNC, see 2.3.3) and after processing sends them to the DAQ system via S-Link. LIBDP card performs the following tasks:

- stores the incoming event data in the level-1 buffer for the latency of the level-1 trigger (~ 1900 events), extracts the event data from the level-1 buffer upon receiving the level-1 trigger decision from the TFC system - discard events, rejected by the level-1 trigger, or retain accepted events for further processing,
- reproduces the algorithm of the level-1 trigger preprocessor (for monitoring and off-line trigger efficiency analysis) and add this information to the output event data,
- performs zero-suppression and detects the clusters,
- (optionally) calculates the pedestals and noise for each of 256 detector channels and communicate them to the ECS system,
- sends non zero-suppressed data to the DAQ system in the special mode of operation or periodically,
- encapsulates the output data and sends them to the DAQ system via S-Link [6],
- interfacing to the ECS controller for parameter setting and monitoring via read/write control interface.

Several possible implementations both for the level-1 buffer (FIFO, DPM, SRAM with controller) and the data processor (DSP, FPGA) will be studied but not all possible combinations are foreseen.

2.6.1 Level-1 buffer

The Level-1 buffer (L1B) is a synchronous dual port memory and logically it's a FIFO. It stores the incoming events for the latency of the level-1 trigger (~1900 events) and it's size is defined as 64K words. L1B may be implemented using real dual port memories (FIFO, DPM) or SRAM with controller. The SRAM based L1B is the most cheap and flexible solution but needs more development efforts. L1B has two ports, write and read.

2.6.1.1 Write port

Data are written into the L1B as a burst of 34 words for one event (2 header words followed by 32 data words, see 2.3.3). The burst frequency is 40 MHz for the data, coming from the FADC card. In the L1B data may be written with 80 MHz from the SyncFPGA, which may allow the data multiplexing (this is not foreseen in the proposed SyncFPGA implementation). The address for the write port is not needed but may be implemented (if necessary for DPM or SRAM), using a simple counter. Writing to the random address is not necessary. The L1B may generate the full flag. This feature is not used during standard data taking mode to generate throttle, because it is done centrally in the Read-out Supervisor.

The following signal are available on the DAQI card write port connector (write clock is the main RB3 board clock):

- input data, DATA_SYNC from four SyncFPGAs, 4 x 32-bit,
- four WRITE_SYNC signals from SyncFPGAs,
- four output L1B full signals,
- reserved signals, 2 per SyncFPGA, 8 in total.

Connection of the FIFO devices is straight forward to this port. Modern DPM devices have auto-incrementing on-chip address counter and also easy connected to this port without external logic. SRAM needs a simple write counter.

2.6.1.2 Read port

Data are read in the burst of 34 words. The burst frequency may be the maximum allowed for the memory device. The "event skipping" mechanism (for the events, rejected by the level-1 trigger) may be useful but is not a requirements. This feature requires advancing of the read counter to the next event in the L1B without reading the data. Reading from the random address is not necessary. Empty flag may be useful for test purposes, but generally the data shall be in the L1B before the reading which starts after level-1 trigger decision.

The read port definition depends on the L1B implementation and is an internal DAQI card issue. The following set of signal may be suggested as a starting point for development (read clock is an internal DAQI clock which can be main RB3 board clock):

- data (4 x 32-bit) and read enable,
- input memory address, 17-bits, to be used in DPM or SRAM L1B implementations,
- empty flag, reset, "skip event" signals.

For the FIFO devices address lines are not used and "event skipping" is not possible. DPM devices may be connected directly, an empty flag may be generated using additional up-down counter, if necessary, and "event skipping" is possible. SRAM devices need a controller with write and read counters, address multiplexer, etc.) but allow flexible access.

2.6.1.3 Level-1 buffer read/write access via ECS

For debugging purposes, L1B may need a read / write access from the ECS system. There are several possibilities which may be considered and tested:

- data may be written into the L1B from the SyncFPGA (in the test mode of operation, using SyncFPGA control interface) and read-out using control interface on the DAQI card,
- full read / write access to the L1B may be provided on the DAQI card from it's control interface

2.6.1.4 Level-1 buffer dump for the test purposes

Level-1 buffer dump during data taking (stop data taking, read entire L1B via ECS, resume data taking) may be problematic for the FIFO L1B implementation (the retransmit possibility of the FIFO devices allows to re-read data only from the first physical location of the FIFO).

DPM and SRAM implementations of the L1B are more flexible and may allow this L1B feature.

2.6.2 Data processor

Each data processor handles 256 detector channels (data from two SyncFPGAs). The main task, executed by the data processor are:

- extracts the event data from the level-1 buffer (upon receiving the level-1 trigger decision) and:
    - reproduces the algorithm of the level-1 trigger preprocessor,
    - performs zero-suppression,
    - formats the output data and sends them to the DAQ interface,
- follows the pedestals and noise for each of 256 detector channels (every ? event),
- sends non zero-suppressed data to the DAQ system in the special mode of operation, periodically or together with zero-suppressed data for several channels (defined by the control register in the DAQI card, accessible by ECS controller.

2.6.3 Link interface

Link Interface sends the formatted data to the DAQ system via DAQ link. The interface to the trigger link is defined as S-Link [6] for the time being without specifying the physical implementation of the DAQ link - S-Link or other type of link.

2.6.3.1 Data format

DAQ link data format consists of DAQ link transport format (link dependant) which contains the VELO detector (or Inner Tracker detector) data itself.

A VELO detector data format (normal data taking with zero suppression) shall have DAQ event identifier(s), DAQ link identifier, 7-bit VELO sensor number (5-bit station number + 2-bit sensor number in station), data type (= '0') and data. The latter may be described as:

- 11-bit VELO detector channel number (= address of the first hit in cluster),
- 3-bit number of hits in the cluster, up to 8 hits,
- 8-bit L1T info (1 bit per hit, '1' = hit was sent to the L1T)

- up to eight 8-bit words (signal height of the hit).

Data format for the non zero-suppressed event data (sent periodically during normal data taking) is indicated by the data type (='1') and differ in data presentation:

- 2048 8-bit words (signal height of detector channel).

Optionally, non zero-suppressed event data may be sent only for a part of the sensor (e.g. for 512 channels) in order to smooth the data load on the DAQ. In this case the sensor part identifier must be included in the data format for the non zero-suppressed event data. (Shall all ODE modules send non zero-suppressed event data for the same event ?).

Data format for the noise / pedestal data is the same as for the non zero-suppressed event data with different data type ('2' - noise, '3' - pedestals). It's not clear, when they should be sent.

Alternatively, non zero-suppressed event data, noise and pedestals (for a small number of channels) may be sent during normal data taking with zero suppression. A VELO detector data format in this case could be: TBD.

2.6.3.2 DAQ link implementation

TBD

2.6.4 TFC interface

For each event, stored in the level-1 buffer, the TFC system provides a yes / no decision from the level-1 trigger. Decisions arrive in the same order as the events are stored in the level-1 buffer. Each decision contain 3-bit trigger type and 2-bit event identifier. Trigger type is defined as following:

Bits <2..0>	Trigger type
0	Discard event
1	Trigger of physics event
2	Random rigger
3	Trigger on empty bunch crossing (single beam)
4	Trigger on empty bunch crossing (no beam)
5	Trigger on calibration pulse
6	Trigger on timing alignment
7	Reserved

Two bit event identifier is two LSB of EVENT_CNT sent by the level-1 trigger interface, LinkFPGA, to the level-1 trigger in the data format (see 2.5.2.2) and stored in the level-1 buffer together with the event data (see 2.3.3). Therefore, from the TFC interface to the DAQI card there are 5 bits of the trigger type and event identification and a strobe.

Two MODE<1..0> bits define the operation mode of the DAQI card.

The output FIFOs in the Link Interface block may overflow. The full flag may be sent out of DAQI card for further processing in TFC interface.

2.6.5 Control interface

Control interface to the DAQI card is a parallel interface from the ECS controller on the main RB3 board. It has to provide the access to the internal registers and memories of the DAQI card:

- download (or change) DSP program and all parameters, which are used to reproduces the level-1 trigger preprocessor algorithm (pedestal and hit threshold LUTs, mask registers) and to execute the zero suppression algorithm and pedestal / noise calculation,
- communicate to the ECS system new parameters for download to the level-1 trigger preprocessor.

The following parameters have to be loaded into DAQI:

- N-bit DAQ link identifier (N - TBD by DAQ group).

2.6.6 DAQI card implementation

TBD

3 Interfaces to control systems

3.1 Timing and Fast Control system interface

The interface to the LHCb Timing and Fast Control (TFC) system contains TTCrx receiver chip [9], front-end emulator and timing/control FPGA. It delivers clock and fast control signals to other parts of the RB3 board. The TFC interface also contain "LHCb standard" control/status registers accessible via ECS controller on the RB3 board. A global RB3 board throttle signal generation/control is also provided by the TFC interface.

3.1.1 TTCrx chip

TTCrx chip provides clock and level-0 trigger accept signals, fast control commands, resets, level-1 trigger decision and 12-bit bunch crossing number (BUNCH_CNT) for the RB3 board. For the RB3 board, a small daughter card with the TTCrx chip is used. Access to the internal registers of the TTCrx chip is provides by the I2C interface on the chip.

3.1.1.1 Main features

The TTCrx recovers 40.08 MHz LHC reference clock which comes out of the TTCrx as Clock40 signal. Two internal independant phase shifters provide a programmable clock delay in steps of 104 ps (Clock40Des1 and Clock40Des2 oupput signals). This feature may be used for a board wide clock phase adjustment relatively to the incoming analog data when Clock40Des1 or Clock40Des2 is used as a main RB3 board clock.

The level-0 trigger accept signal (L1Accept ouput of the TTCrx chip) can be delayed in steps of 25 ns (one clock cycle) up to 15 clock cycles. This signal is used in the front-end emulator and delay shall be set to the same value as in the front-end chips. This signal is also counted in the timing/control FPGA by the 24-bit event counter (EVENT_CNT) for event identification purposes in the SyncFPGA.

Two - 12-bit bunch and 24-bit event - counters are available in the TTCrx but only bunch counter is used in the LHCb environment (event counter is implemented in the timing/control FPGA). The bunch counter is free-running, incremented by the clock and can be reset by TTCrx broadcast command. Its content is available on the BCnt<11..0> pins during the level-0 trigger accept signal together with BCntStr strobe signal. Reset signal (BCntRes) is also available on the output pin and can be use in the timing/control FPGA for orbit counting (ORBIT_CNT).

In the LHCb environment TTCrx 8-bit broadcast commands are used to distribute fast control commands, resets and level-1 trigger decision. The allocation of the 8 available bits is the following:

<table>
<tr><th>LHCb command</th><th><7></th><th><6></th><th><5></th><th><4></th><th><3></th><th><2></th><th><1></th><th><0></th></tr>
<tr><td>Noop</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Command</td><td>0</td><td>0</td><td colspan="2">CMD<1..0></td><td>X</td><td>X</td><td rowspan="3">Event counter reset</td><td rowspan="3">Bunch counter reset</td></tr>
<tr><td>Reset</td><td>0</td><td>1</td><td colspan="2">Reserved</td><td>L1 reset</td><td>L0 reset</td></tr>
<tr><td>L1 trigger decision</td><td>1</td><td colspan="4">L1 trigger type</td><td colspan="2">LSB of event counter</td></tr>
</table>

Bits <1..0> are reserved for the bunch counter and event counter reset in the TTCrx and also available as BCntRes and EvCntRes strobes on the TTCrx output pins.

Bits <7..6>="00" indicate a fast command (their use for the RB3 and the final readout board is not yet defined) and bits <7..6>="01" indicate a reset commands - together with the bits <3..2> - level-0 or level-1 reset.

Bit <7>='1' indicates the level-1 trigger decision. In this case, bits <6..4> define the trigger type and bits <3..2> are the two LSBs of the event counter (which counts level-0 accepts). Trigger type <6..4>="000" is a level-1 trigger reject while other combinations are different types of accepted level-1 triggers which may need different actions in the data processor (L1DBP).

3.1.1.2 TTCrx test board

The last radiation-hard DMILL version of the TTCrx chip is packaged in a 144 pin BGA 13 mm side package. The TTCrx test board contains TTCrx chip, a photodiode and a serial configuration PROM. It supports the use of pull up/down resistors to set the TTCrx individual address and operation mode during initialization in a case when the PROM is not used. The card size is 66 mm x 64.8 mm. Pin assignment for the test board connectors J1 and J2 is shown below:

Connector J1

Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
Clock40	1	2	Clock40Des1	Dout<2>	27	28	Dout<3>
Brcst<5>	3	4	Brcst<4>	Dout<4>	29	30	Dout<5>
Brcst<3>	5	6	Brcst<2>	Dout<6>	31	32	Dout<7>
Clock40Des2	7	8	BrcstStr1	Reset_b	33	34	TTCReady
DbErrStr	9	10	SinErrStr	GND	35	36	GND
SubAddr<0>	11	12	SubAddr<1>	GND	37	38	GND
SubAddr<2>	13	14	SubAddr<3>	GND	39	40	GND
SubAddr<4>	15	16	SubAddr<5>	GND	41	42	GND
SubAddr<6>	17	18	SubAddr<7>	GND	43	44	GND
DQ<0>	19	20	DQ<1>	GND	45	46	GND
DQ<2>	21	22	DQ<3>	GND	47	48	GND
DoutStr	23	24	GND	GND	49	50	GND
Dout<0>	25	26	Dout<1>				

Connector J2

Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
BrcstStr2	1	2	ClockL1Accept	SDA	27	28	JTAGTDI
Brcst<6>	3	4	Brcst<7>	BCntStr	29	30	Serial_B_Channel
EvCntRes	5	6	L1Accept	GND	31	32	GND
EvCntLStr	7	8	EvCntHStr	GND	33	34	GND
BCntRes	9	10	GND	PIN Preamp VCC	35	36	PIN Preamp VCC
BCnt<0>	11	12	BCnt<1>	PIN Preamp VCC	37	38	PIN Preamp VCC
BCnt<2>	13	14	BCnt<3>	N.C.	39	40	SCL
BCnt<4>	15	16	BCnt<5>	GND	41	42	GND
BCnt<6>	17	18	BCnt<7>	TTCrx VDD	43	44	TTCrx VDD
BCnt<8>	19	20	BCnt<9>	TTCrx VDD	45	46	TTCrx VDD
BCnt<10>	21	22	BCnt<11>	GND	47	48	GND
JTAGTMS	23	24	JTAGTRST_b	GND	49	50	GND
JTAGTCK	25	26	JTAGTDO				

3.1.1.3 TTCrx control interface

The TTCrx chip contains a total of 20 user-accessible 8-bit registers. The I2C interface is used to read and write (or reset) all the registers. After a write access, the corresponding register is, in general, set to the value of the transmitted data byte. However, writing into the counter registers resets them. Writing the value 5 into the status register initiate a reset procedure and writing the value 0 into the status register deletes the watchdog-reset flag.

All data transfer over the I2C bus is performed using only two I2C registers: the I2C_pointer register and the I2C_data register. The I2C_pointer register is 5 bits wide and contains the address of the internal TTCrx register as defined in Table 3. The I2C_data register is used to read or write data from/to the internal TTCrx register, addressed by the I2C_pointer register. Hence each I2C access is performed in two steps: write the TTCrx internal register number in the I2C_pointer register and then read or write the I2C_data register.

The I2C_pointer and I2C_data registers occupy two consecutive positions in the 7 bit I2C address space. The upper 6 bits of the 7 bit I2C address are defined in the TTCrx ID_I2C<5:0> base address register and are initialised during a reset.

3.1.2 FE emulator

The real BEETLE or SCTA_VELO chip is used as the front-end emulator. For this application it is packaged in such a way that only control and output signals are used. The analog output signals are converted to the logic levels using comparators.

3.1.2.1 BEETLE chip

The BEETLE chip is 128-channels front-end chip with 160 stages analog pipeline, 16 stages derandomizer and 4 output multiplexers with 40 MHz read-out speed. All digital control and data signals are LVDS. Three signals are used to drive the chip:

- Clk - this is a system clock, all operation are synchronous to the Clk and all inputs are sampled at the rising edge of the Clk, unless otherwise noted.
- Trigger - this signal is used to send triggers to the chip (when it is in a “Busy” mode) or to program the chip.
- Reset - this signal has two functions: indicating arrival of programming data via trigger input (if Reset signal is active for exactly one Clock cycle) and resetting the chip (if it is active for two or more Clk cycles).
    - “Soft reset” (Reset is active for 2 Clk cycles) - resets write and trigger pointers, read-out process is not disturbed,
    - “Hard reset” (Reset is active for 3 Clk cycles) - resets all pointers and switchs chip into “Busy” mode when it accepts triggers,
    - “Power up reset” (Reset is active for 4Clk cycles or longer) - resets pointers and all internal registers and switchs chip into “Idle” mode when it has to be programmed.

An on chip error (which ?) is indicated by notError open drain output. Two pins (T1A and T1B) are used to generate the chip address for programmming via reset/trigger or I2C interface. Four BEETLE chip AnalogOut signals are synchronous to the clock. First two slots carry a header - pipeline column number or the internal state of the chip in a case of error condition (TBD). DataValid signal indicates the presence of valid data on the AnalogOut outputs.

There are 34 internal 8-bit registers on the BEETLE chip which are programmable via I2C interface from the RB3 board ECS controller. Only those internal registers, which are responsible for the chip control/readout, shall be programmed in the same way as the front-end chips on the detector.

3.1.2.2 SCTA_VELO chip

TBD.

3.1.2.3 Front-end emulator card

The front-end emulator implemented on a daughter card which contains the front-end chip (BEETLE or SCTA_VELO), TTL to LVDS converters, comparators for the output analog signals (to convert the 4 analog signals into 4 pseudo-digital bits) and +5V/+2.5V power regulator. The card interface is as following:

- Inputs: Clock, Trigger, Reset- TTL, SCL, SDA - CMOS,
- Outputs: DataOut<3..0>, DataValid, notError - TTL,
- Power: +5V (xx pins), GND (xx pins)

The front-end emulator is driven by the clock and level-0 trigger accept signals from the TTCrx chip. The latency of the level-0 trigger accept signal shall be equal to one for the front-end chips (adjusted in the TTCrx chip, if needed).

The reset is generated in the timing/control FPGA from different reset signals for the RB3 board. I2C interface to the front-end emulator is provided by the ECS controller on the main RB3 board.

3.1.3 Timing/control FPGA

The timing/control FPGA in the TFC interface provides event identification and global RB3 reset and control logic.

- Event identification block - this block provides 8-bit orbit counter (ORBIT_CNT) and 24-bit event counter (EVENT_CNT). It also adjust latency of the front-end emulator output data, generates PCN_FEE and PCN_VALID from DataOut<3..0> and DataValid signals, and perform time alignment of all event identificatin information for SyncFPGA.
- Board control block - this block provides decoding logic for the TFC fast control commands, generation of different resets for the RB3 board (front-end emulator reset, global RB3 resets), “LHCb standard” control/status registers (the board type identifier, serial number, hardware revision number, “status”/”ready” bit, “reset” bit, etc.) and the board modes of operation.
- RB3 throttle generation.
- Control interface - provides interfacing to the ECS controller for parameter setting and monitoring.

3.1.3.1 Event identification block

This block contains different counters, PCN_FEE generation and time alignment circuits.

- Event conter (EVENT_CNT) - it counts level-0 trigger accept signals, reset by EvCntRes signal from the TTCrx and may be read via control interface.
- Orbit counter (ORBIT_CNT) - it counts BCntRes signals, reset by flobal RST signal and may be read via control interface.

- Bunch counter value from TTCx chip is loaded in the internal register using BCntStr signal and may be read via control interface.

Writing to these counters / register resets them (this feature is disabled during normal mode of operation and enabled during test mode). 8-bit PCN_FEE value and PCN_VALID signal are generated from DataOut<3..0> and DataValid signals and aligned in time with the other counter / register values before transmitting to the SyncFPGA.

3.1.3.2 Board control block

- TFC fast control command decoding logic - decodes TTCrx 8-bit broadcast commands, level-1 trigger decisions are sent to the data processor (DAQI card), level-0 and level-1 resets are sent to the reset generation logic.
- Reset generation logic - receives level-0 and level-1 resets from TFC, external reset from the main RB3 board (OR of the power-up reset, front panel push button reset, reset signal from the LHCb custom power distribution backplane and the front panel NIM input reset) and the internal reset from the “LHCb standard” control register (accessible from ECS controller). It generates front-end emulator reset (from the TFC level-0 reset) and global RB3 board reset.
- “LHCb standard” control / status registers - the board type identifier, serial number, hardware revision number - accessible from ECS controller. The global RB3 board control / status register has two MODE bits (normal and test modes) and BoardReady bit.

3.1.3.3 RB3 board throttle generation

All individual throttle signal (or full flags) from different location on the RB3 board are handled in the timing / control FPGA. They can be individually disabled. A global “OR” of all individual throttles is generated and made available as a NIM signal on the LEMO connector on the front panel.

3.1.3.4 Control interface

The following parameters have to be loaded into timing / control FPGA:

- BUNCH_CNT, EVENT_CNT, ORBIT_CNT, PCN_FEE, alignment parameter,
- front-end emulator reset mode, control / status registers,
- throttle mask.

Access to these two control registers is possible via two external interfaces - parallel and I2C, implemented for the evaluation purposes in order to choose the final one.

3.1.3.5 Timing/control FPGA pin count and possible device

Signal	N pins	in/out	Int FPGA Src/Dst	Ext Blk
Level-0 trigger accept (L2Accept), EvCntRes	1+1	in	Event identification	TTCrx
BCnt<11..0>, BCntStr, BCntRes	12+1+1	in	Event identification	TTCrx
DataOut<3..0>, DataValid	4+1	in	Event identification	FEEm
BUNCH_CNT, EVENT_CNT, ORBIT_CNT	12+24+8	out	Event identification	SyncFPGA
PCN_FEE, PCN_VALID	8+1	out	Event identification	SyncFPGA
Brcst<7..2>	6	in	Board control block	TTCrx
L1_DECISION, L1D_STROBE	5+1	out	Board control block	DAQI card

Signal	N pins	in/out	Int FPGA Src/Dst	Ext Blk
EXT_RST	1	in	Board control block	main
FEEm_RESET, RST	1+1	out	Board control block	FEEm, main
MODE	2	out	Board control block	main
THROTTE_IN	?	in	Throttle	main
THROTTLE_OUT	1	out	Throttle	Connector
SDA, SCL (I2C interface)	1+1	inout+in	Control interface	ECS
[A4..A1] (I2C chip select)	4	in	Control interface	h/w pins
DATA_ECS, AD, CS, WR	8+3	inout	Control interface	ECS
CLK_MAIN	1	in	Internal logic	TTCrx
Total	110+?			

Altera APEX.

3.1.3.6 Timing/control FPGA configuration

Configuration of the timing/control FPGA is similar to the SyncFPGA (see 2.3.7).

3.2 Experiment Control System interface

The interface to the LHCb Experiment Control System on the RB3 board (ECS controller) shall provide:

- read / write access to internal registers inside FPGAs and memories (LUTs, RAMs, EEPROMs) inside and outside of FPGAs,
- read / write access to the internal registers of the other components on the board,
- on-board FPGA configuration (directly or via EEPROM re-programming).

The RB3 ECS controller has to interact from one side with the components on the RB3 board and from other side with the LHCb ECS "master". The on-board interfaces are defined for some "standard" components and have to be implemented for others. Software on ECS controller and ECS "master" will allow read / write I2C / JTAG / ParallelBus interfaces, support component definition, etc.

3.2.1 ECS controller

ECS interface on the RB3 board is implemented is a way, which allows evaluation of different ECS controllers. "LHCb standard" ECS controllers with local intelligence, which can be used in the counting room, are: credit-card-PC (CC-PC) based ECS controller and CAN / ELMB controller. At the initial stage of the RB3 board debugging a controller from EIG may be used.

3.2.1.1 Credit-Card-PC (CC-PC) based ECS controller

The main features of the CC-PC based ECS interface are:

- based on SMART credit-card PC with all interfaces (MachZ processor),
- board space required: 50.00 mm x 66.00 mm,
- cost estimate - 350 CHF,
- "LHCb standard" 240-pin connector, type (?),
- interfaces: parallel bus (32 address / data, 11 control lines), 4 x I2C, 2 x JTAG,
- connection to ECS "master" - Fast Ethernet (TCP / IP), star topology,

3.2.1.2 Embedded Local Monitor Board with CANbus interface (CAN/ELMB)

The main features of the CAN / ELMB based ECS interface are:

- based on two micro controllers - AVR ATmega103 and AT90S2313,
- board space required: 85.00 mm x 123.00 mm,
- cost estimate - 150 CHF,
- connectors - 2 x 40-pin,
- interfaces: I / O pins - 8 in, 8 out, 18 in / out, software configured as parallel bus, I2C or JTAG,
- connection to ECS "master" - CAN serial bus - CAN controller SAE81C91.

3.2.1.3 EIG controller

- based on micro controller
- board space required - 71.00 mm x 117.00 mm,

- cost estimate - ?,
- 50-pin connector,
- interfaces: I2C. JTAG, parallel (?),
- connection to stand-alone PC (not an ECS “master”) - RS232 or CANbus.

3.2.2 Interfaces to the devices on the board

3.2.2.1 I2C interface

The following components in the RB3 board need I2C interface from the ECS controller:

- DAC chip (2 in total), PHOS4 chip (4 in total), TTCrx chip, BEETLE chip,
- SyncFPGA (4 in total on the RB3 board, 16 - on the final), timing/control FPGA,

3.2.2.2 JTAG interface

The following components in the RB3 board need JTAG interface from the ECS controller:

- FPGA configuration EEPROMS, 4 in total (for Sync, Prep, Link and timing/control FPGAs)

3.2.2.3 Paralel interface

The following components in the RB3 board need Parallel interface from the ECS controller:

- PpFPGA, LinkFPGA, (optionally SyncFPGA and timing/control FPGA), DAQI card.

4 Main board

The main board is a 9U module (366.70 mm x 400.00 mm, IEEE1101.10 mechanics) and occupies two slots in the crate (because of the daughter cards for some parts of the board). Board power is provided by the LHCb custom power distribution backplane in J3 position in the crate. The daughter cards on the main board are:

- four 4-channel FADC daughter cards,
- one TTCrx test board with the TTCrx chip, a photodiode and a serial configuration PROM,
- one front-end emulator card with the front-end chip,
- one level-1 buffer, data preprocessor and DAQ interface card (DAQI card),
- two S-Link physical Link Source Cards, one for the level-1 trigger and one for the DAQ interfaces,
- one (out of several possible) ECS controller card.

The physical links and to the external systems are:

- optical link from the TFC system to the photodiode on the TTCrx test card,
- LEMO connector for the RB3 Throttle output NIM signal,
- 16 data transmission links (e.g. twisted pair analog links),
- two S-Links - one to the level-1 trigger and one to the DAQ system,
- ECS controller link (Fast Ethernet, RS232 or CANbus, depending on the controller implementation),
- LEMO connector for the RB3 Reset input NIM signal,

4.1 Board resets

The reset signals for the RB3 board can be generated from several sources:

- local reset of the RB3 board on power-up (?) or via front panel push button (?),
- remote resets generated by the TFC system (level-0 and level-1 resets), by the ECS controller, by the LHCb custom power distribution backplane (generated by ?) or via front panel NIM input (?).

The reset actions may be global for the RB3 board. They are initiated by (power-up, push button, NIM input,) backplane, TFC level-1 reset and ECS global reset. Individual parts of the RB3 board can be reset via their control interfaces from the ECS controller. TFC level-0 reset only resets the front-end emulator.

Reset signal for FPGAs may be send only after termination of their configuration (and, therefore, power-up reset may be not useful).

4.2 Operation modes

There are two operation modes of the RB3 board:

- Normal run mode - the board accepts the input data from the front-end electronics, performs data preprocessing for the level-1 trigger and data processing for the DAQ system under control of the TFC and ECS systems. Zero suppression in the data processing part may be set in different modes: full, partial and no zero suppression.

- Test mode - the input data are received from the input test memories (input FIFOs in the SyncFPGAs).

4.3 Board operation

On order to operate the RB3 board, the following external system (or their emulators) will be needed:

- TFC system - it can be emulated by the TTCvi and TTCvx modules, both VME 6U modules (therefore a 6U VME crate with a crate controller - embedded VME CPU or PC with a VME interface - is necessary to drive the TFC emulator),
- DAQ system and level-1 trigger system - they can be emulated by the S-Link receivers - Link Destination Cards - housed in the PC (PCI cards) or in the embedded VME CPU (PMC cards),
- ECS system - a PC may be used as a LHCb “master”.

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