The LHCb Trigger and Readout (1)

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on behalf of the LHCb Collaboration

The LHCb experiment

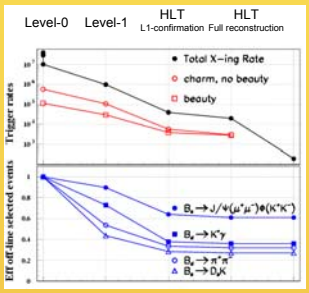
The LHCb detector is a single-arm spectrometer which will study the B-mesons produced in p-p collision in the LHC collider at CERN starting from 2007.

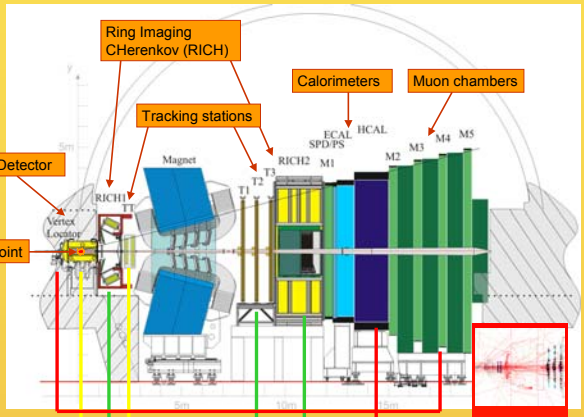
Physical features

- Luminosity: $L = 2 \cdot 10^{32}\ cm^{-2}\ s^{-1} = 200\ \mu b^{-1} s^{-1}$
  -10÷50 times lower than @ATLAS, CMS
- $\sigma_{total} \cong 100\ \mu b$, $\sigma_{inel} \cong 80\ \mu b$, $\sigma_{vis} \cong 60\ \mu b$
  - visible events ≡ at least 2 tracks in acceptance
  * 12 MHz total (visible) interaction rate
  * 10 MHz total (visible) event rate (pile-up)
- Assumed $\sigma_{bb} \cong 500\ \mu b$
  * 200 kHz bb event rate
  - 15 kHz: one B decay product in the acceptance
  * 800 kHz cc event rate
- But low branching fractions! Expect (offline reconstructable events):
  * $B_d \to J/\psi(\mu^+\mu^-)\ K_S(\pi^+\pi^-)$ 1 per minute
  * $B_d \to \pi^+\pi^-$ 1 in two minutes
  * $B_s \to D_s(K^+K^-\pi^-)\ K^+$ 1 in six minutes
  * $B_s \to \mu^+\mu^-$ 1 per week (?)

The trigger

LHCb features a **three-level trigger** system to bring down the rate of visible p-p interaction (10 MHz) to a few KHz, at which rate events can be stored for further analysys. The trigger levels are called Level-0 (**L0**), Level-1(**L1**) and High Level Trigger (**HLT**).



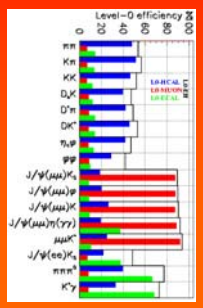


10 MHz
p-p visible interactions

L0-Trigger (L0)

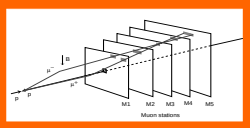
- Fully synchronous and pipelined hardware trigger (custom electronics) with fixed latency (4 μs);
- **Global event variables** (10MHz→ 7MHz) to reject:
  - multiple primary vertices (Pile-up) events, too hard to reconstruct and that don't enrich the signal content,
  - too complicated events (Pile-up+SPDs),
  - 'empty' events (HCAL),

  to reduce background from halo-muons;
- **B signatures** (7Mhz→ 1MHz):
  - high p_t muons (Muon),
  - high E_t electrons, photons, π^0 (ECAL),
  - and hadrons (HCAL).



	Rate (kHz)
Hadron	705
Electron	103
Photon	126
π^0 local	110
π^0 global	145
Muon	110
Di-muon Σp_T^{μ}	145

	bb (kHz)	cc (kHz)
Generated	165	840
After L0	30	106

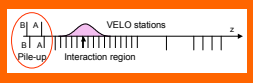


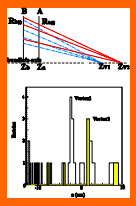
Muon Trigger

- Straight line search in M2-M5,
- extrapolation to compatible hits in M1,
- momentum measurement ($\Delta p/p$~20% for b-decays),
- Sends 2 highest Pt muon per quadrant to L0 Decision Unit.

Pile-up system

- 2 VELO sensor measuring R (before interaction point),
- produce histo of Z (along beam axis) from hits in the 2 planes,
- PID from HCAL,ECAL,PS+SPD
- Sends to L0 decision Unit the # of tracks in the second peak + hits multiplicity





Calorimeter Trigger

- Look for high E_t candidates in regions of 2x2 cells (6000 in ECAL, 1500 in HCAL),
- PID from HCAL,ECAL,PS+SPD
- Sends to L0 decision Unit the highest E_t candidate for each type, and global event variables such as total energy and SPD multiplicity.

Level-0 Decision Unit

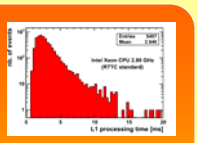
- OR of high E_t candidates,
- applies cuts on global variables.

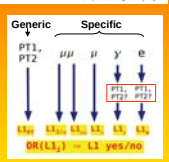
Pile-Up, Muon, Calorimeters

1 MHz

L1-Trigger (L1)

- Software trigger with maximal latency of 52.4 ms (max L1 accept rate: 40 KHz),
- Parallel and overlapping subtriggers:
  - Generic line (to enhance b content)
    - L1-Variable: log (PT1)+log(PT2), IP > 0.15 mm,
  - Photon and electron lines:
    - L1-Variable (relaxed) + ECAL > 3.4 GeV (e)
      3.1 GeV (γ)
  - Muon lines:
    - Single muon: PT > 2.3 GeV, IP > 0.15 mm,
    - Di-muons:
      - m(μμ) > m(J/ψ) - 500 MeV OR
      - m(μμ) > 500 MeV, IP > 0.05 mm.
- Final decision is OR of all subtriggers.





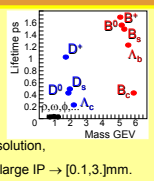
	Rate (kHz)
Generic	29.2
Single-muon	3.2
Di-muon	1.4
Di-muon J/ψ	0.6
Electron	2.3
Photon	2.3

L1 Efficiency	
$B_d \to \pi^+\pi^-$	83%
$B_s \to D_sK$	81%
$B_d \to D^0K^*$	85%
$B_s \to K^*\gamma$	67%
$B_s \to J/\psi(\mu^+\mu^-)\ \phi$	87%

	bb (kHz)	cc (kHz)
Generated	165	840
After L0	30	106
After L1	6.4	7.2

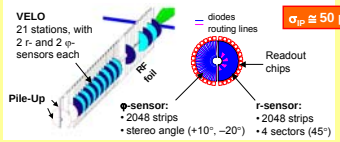
L1 generic trigger strategy

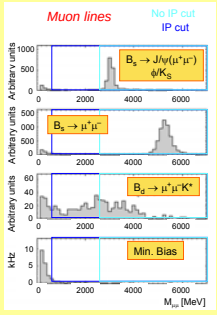
- B hadrons are heavy and long lived,
- look for high impact parameter (IP) and p_t tracks.



IP measurement (VELO):

- Fast 2D tracking (r-z) provides good resolution,
- 3D tracking (add φ) only for tracks with large IP → [0.1,3.]mm.



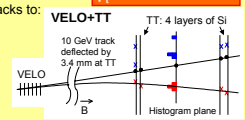


p_t measurement:

extrapolation of VELO tracks to:

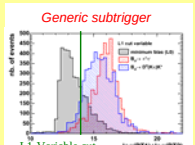
- TT hits,
- L0-objects (muons).

p_t resolution: 20–40%



p_t resolution	6%
Matching eff.	91%
Purity	51%

← VELO+L0 muons



VELO,TT, L0 info

40 KHz

High Level Trigger (HLT)

- Software trigger with 2 kHz accept rate;
- Generic HLT (to reduce the rate to 10 kHz), partial reconstruction (IP,PT):
  - Redo L1algorith (with better IP and PT resolution),
  - High rate muons (IP and PT to identify μ and J/ψ).
- HLT specific (to reduce the rate down to 2 kHz), full reconstruction and PID :
  - Fast Inclusive (1.8 kHz)
    - easy → robust;
    - un-biased sample → trigger on *the other B*;
    - for channels uncovered by exclusive selections.
  - Exclusive (200 Hz) selections for LHCb hot physics.

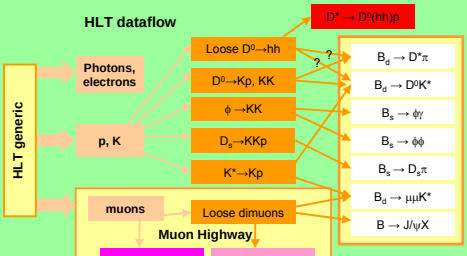
HLT algorithms are still *work in progress*: especially better tracking is under study.

	bb (kHz)	cc (kHz)
Generated	165	840
After L0	30	106
After L1	6.4	7.2
After HLT Gen	3.8	2.7

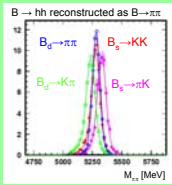
	Rate
Generic HLT	13 kHz
Inclusive B	850 Hz
D*	250 Hz
Dimuon	660 Hz
Exclusive B	260 Hz

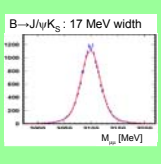
HLT Efficiency	
$B_{d,s} \to h^+h^-$	88%
$B_s \to D_sh$	62%
$B_d \to D^*\pi$	55%
$B_s \to \phi\gamma$	62%
$B_d \to K^*\mu^+\mu^-$	91%
$B_s \to \mu^+\mu^-$	98%

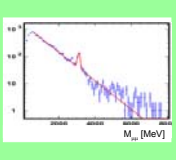
HLT dataflow



All recostructed B masses ~ 30 MeV resolution







Conclusions

While L0 has been finalized and is in production right now, L1/HLT algorithms are still in development, to match our evolvement in understanding LHCb physical potential.

The final aim is a simple, flexible and robust trigger system, that relies on redundancy (more than one path to trigger an event) for highest possible efficiency

All detector data

≤2 KHz

Event rate

Storage

The LHCb Trigger and Readout (2)

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The LHCb DAQ

Inside the cavern: L0 electronics

- very high radiation levels (from 1 Mrad to 10krad) around the LHCb detector require radiation hard equipment (rad hard ASICs, antifuse based FPGAs but no SRAM based memories);
- each subsystem employs its custom FE electronics;
- only the necessary processing:
  - preamplification,
  - digitization (except for the VELO),
  - storing during L0 latency,
  - transmission over long cables to the counting house;
- synchronization and timing alignment are major issues.

50-100 m long cables

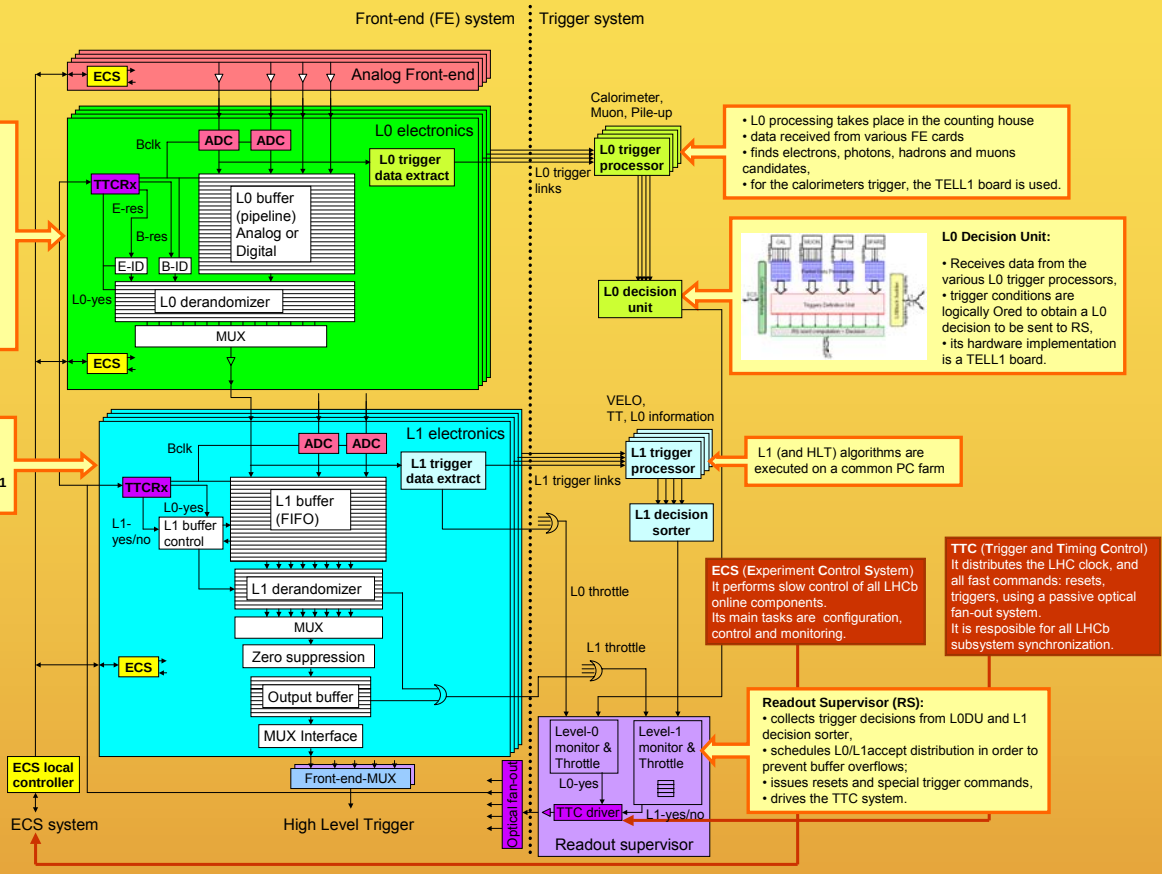
In the counting house: L1 electronics

- Radiation-safe area, so standard electronics can be used;
- all subdetectors but the RICH are using the common **TELL1** board (see box below);

General electronics architecture:

For each trigger level, it consists of:
- some data processing (digitization, zero-suppression,...);
- a buffer defined by the trigger latency;
- an output buffer to derandomize the data transmission to the next trigger level.
- an interface to receive the trigger decision.

Electronics requirements	L0	L1
Latency	fixed (4 μs)	Variable (*ave* = 1ms, *max* = 58 ms)
Maximum output rate	1.1 MHz	40 KHz
Buffer size (evts)	160	58254
De-randomizer depth	16 evts	Min 2 MEPs



- L0 processing takes place in the counting house
- data received from various FE cards
- finds electrons, photons, hadrons and muons candidates,
- for the calorimeters trigger, the TELL1 board is used.

L0 Decision Unit:

- Receives data from the various L0 trigger processors,
- trigger conditions are logically Ored to obtain a L0 decision to be sent to RS,
- its hardware implementation is a TELL1 board.

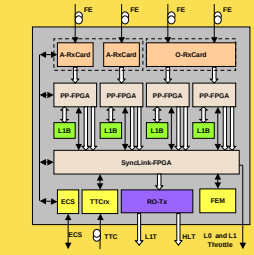
L1 (and HLT) algorithms are executed on a common PC farm

ECS (Experiment Control System) It performs slow control of all LHCb online components. Its main tasks are configuration, control and monitoring.

TTC (Trigger and Timing Control) It distributes the LHC clock, and all fast commands: resets, triggers, using a passive optical fan-out system. It is resposible for all LHCb subsystem synchronization.

Readout Supervisor (RS):
- collects trigger decisions from L0DU and L1 decision sorter,
- schedules L0/L1accept distribution in order to prevent buffer overflows;
- issues resets and special trigger commands,
- drives the TTC system.

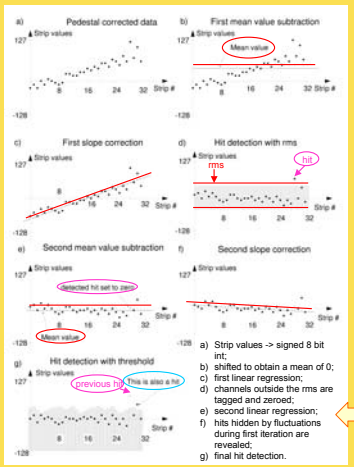
The TELL1 readout board



The TELL1 is an FPGA based board made to readout the data accepted by the L0 trigger and output them, after some processing, to L1 and HLT. It will be used by all LHCb subdetector but the RICH (see brown box on the right). Specific detector needs are accomplished by mezzanine cards while FPGAs allow the necessary flexibility for different data processing. Advantages of having a common board are the reduced development and maintainance costs, and software reuse for all common interfaces.

TELL1 dataflow

TELL1 accepts L0 accepted data as input. After a first synchronisation, the dataflow is split. For the L1 data path, zero suppression is applied and processed data are sent to the L1 PC farm. For the HLT data path, raw data are stored in the L1 buffer and, if the event is accepted, zero suppressed and sent to HLT. The interface to the event building network is provided by four Gigabit Ethernet links.



L0 data input

→ to cope with two different link systems, either 24 x 1.6 Gbit/s high speed optical links (O-Rx card) or 64 x analog copper links (A-Rx card) are accepted as input.

L1 zero suppression and preprocessing

→ cable compensation with FIR filter (VELO),

→ gain correction,

→ pedestal following and correction,

→ channel reordering and masking,

→ common mode suppression,

→ clustering (position calculation with weighted average),

→ linking,

→ in PP-FPGAs.

Common Mode Suppression

For silicon detectors the algorithm implemented in the PP-FPGAs will perform a linear common mode correction:

Noise in channel i $Y_i = a + b \cdot i$

L1 buffering

→ 58254 events stored in DDR SDRAM (96MB).

→ The DDRs are operated at 100MHz, to obtain a write bandwidth of 10 Gbit/s.

HLT zero suppression

→ Once a L1 accept is received, the corresponding event is read from the L1 buffer, zero suppressed, and linked to be sent to HLT (SyncLink-FPGA).

Timing and control interfaces

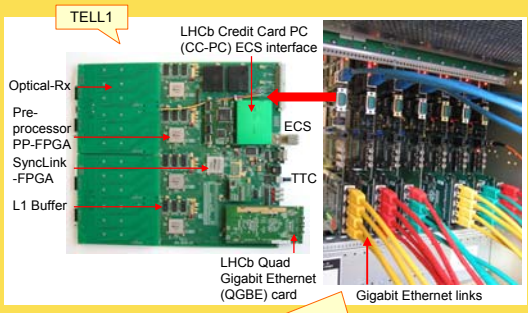
→ TTC and ECS are used respectively for fast and slow control of the board.

Event building network

→ IP over Gigabit Ethernet.

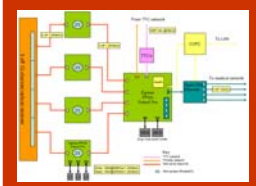
→ Several events are packed into one MEP (Multi Event Packet), allowing moderate packet rates of 40 to 50 KHz.

→ The number of events per MEP can be adjusted for optimal packet size to tune the network traffic.



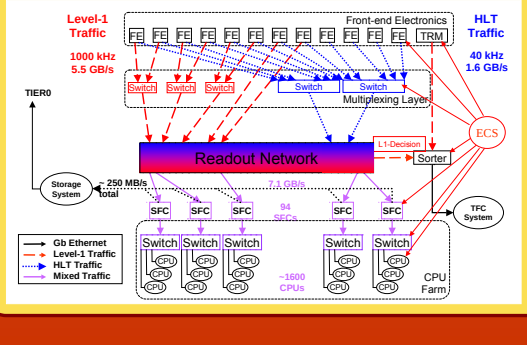
Back plane view of a rack equipped with several TELL1 boards in Lausanne lab. Up to now 20 boards have been produced and tested. Final production (~350 boards) will start in 2006

The RICH readout board



Compared to "standard" TELL1 readout, the RICH:
- does not foresee L1 trigger interface;
- binary readout: more input channels → less processing power needed.

The RICH readout board will however have all requested functionalities to fit into LHCb readout scheme:
- gets data from detectors, from up to 48 optical links, de-serialises, zero-suppresses, etc…
- is controlled by LHCb CC-PC ECS interface,
- data sent out by LHCb 4 Gigabit Ethernet links (QGBE).



L1 & HLT PC farm

- Both L1 and HLT algorithm are executed on the same farm of commercial PCs.
- They share:
  - Ethernet network,
  - Sub-farm controllers,
  - Computing nodes;
- It is flexible and scalable:
  - In depth: more CPUs (<2200),
  - In width: more detector in L1;
- L1 task has priority, while HLT & reconstruction run in background.
- CPU share:
  - L1 ~ 55%,
  - HLT ~ 25%,
  - Reconstruction ~ 20%.

Real Time Trigger Challenge (RTTC)

NOW !!

- *When?*
  - June - July 2005
- *Why?*
  - Test one (or few) subfarms of the DAQ under realistic conditions:
    - Full-speed data path (from simulated detector output to storage)
    - Long-term operation (hours)
    - Test realistic Level-1/HLT code
    - Measure realistic overheads
  - Performance rescaling
    - 'modern' CPUs compared to (today's) standard CERN
  - Test controlling: Monitoring, conditions DB, Farm control, etc.
- *What?*
  - One (or two) racks of 46 CPUs
  - 2-4 Sub Farm Controllers (SFC)
  - RTTC data (one disk server for input/one for storage):
    - 10^7 Level-0 YES, 400k Level-1 YES events, 20k HLT yes
    - Event fragments organized in MEPs