Vertex Detector Electronics: ODE to ECS Interface

LHCb Technical Note

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Abstract

This document describe an interface of the LHCb Vertex Detector Off-Detector Electronics (ODE) to the LHCb Experiment Control System (ECS).

Document Status Sheet

Table 1 Document Status Sheet

1. Document Title: Vertex Detector Electronics: ODE to ECS interface			
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Glossary

I2C Inter-IC Control bus, a two-wire bus for providing a communication link between integrated circuits from Philips Semiconductors.

JTAG Joint Test Action Group, IEEE Std. 1149.1_1190 describing the Test Access Port (4-pins serial port) and Boundary Scan Architecture.

1 Introduction

Vertex detector Off-Detector Electronics (ODE) has to be connected to the LHCb Experiment Control System (ECS) for configuration, control and monitoring. The ODE divided in two sections:

- ODE front-end section in the cavern - (O)100 custom electronics boards and the infrastructure (racks, crates, power supplies, fans).
- ODE processing section in the counting room - commercial boards and systems.

We are discussing in this note only interfacing of the custom ODE boards to the ECS. The interface to the ECS for the ODE cavern infrastructures and the ODE processing section is briefly discussed and the end.

1.1 LHCb ECS

The LHCb ECS has several layers of hierarchy:

- At the top level there is a SCADA (Supervisory Control And Data Acquisition) system, which provides LHCb-wide high level services, normally running on PCs connected by a LAN.
- In the middle there are ECS sub-detector controller(s) providing the integration of each sub-system with the higher levels but also stand-alone control, for tests, debugging and monitoring of the sub-system. This layer can be implemented also by PCs running either (parts of) the SCADA system or servers (like OPC) that communicate with the SCADA system above.
- On the bottom level there are hardware components (electronics boards, power supplies, sensors, etc.). Each hardware component will have an interface to the sub-detector controllers (the interface can vary from low speed field buses for simple devices like sensors to, for instance, ethernet for power supplies). For what concerns electronics boards a similar solution is being envisaged, i.e., to connect each board to either a field bus (e.g. FireWire, IEEE 1394) or to Ethernet. This solution is being evaluated in terms of price and software effort as a replacement for the “HEP standard” VME type solution.

The LHCb ECS group is responsible for:

- The development and deployment of the SCADA framework to be used at the top level and at the sub-controller levels.
- Providing servers (OPC) or server templates to access standard hardware components, i.e. the ones that comply to the interfaces that will be recommended.

The sub-detector groups are responsible for:

- Implementing the recommended hardware interface on their boards.
- Providing the detailed description of the devices to be controlled (i.e the description of the board components) with the help of SCADA framework tools.

- Providing the hardware specific software to be filled-in the server templates.

1.2 ODE board

ODE board will be implemented using a (undefined yet) mechanical and electrical “LHCb standard”. Each ODE board is a self-contained unit with all interfaces to other systems (Front-end electronics, TFC, Trigger, DAQ, ECS). The majority of the board logic is implemented in the FPGAs - Altera, Xilinx or alike. There are also static memories and some other components, like the TTCrx chip and the programmable delay chip (from CERN microelectronics group) and FPGA configuration EEPROMs. The ODE-ECS interface shall provide a possibility of:

- Read / write access to internal registers inside FPGAs and memories (LUTs, RAMs, EEPROMs) inside and outside of FPGAs.
- Read / write access to the internal registers of the other components on the board.
- On-board FPGA configuration (directly or via EEPROM re-programming).

The ODE-ECS controller on the ODE board has to interact from one side with the components on the ODE board and from other side with the ECS sub-detector controller.

The on-board interfaces are already defined for some components (e.g. I2C interface [1] for the TTCrx chip and the programmable delay chip, JTAG interface [2] for the configuration device) and has to be defined for others. To implement an interface protocol a commercial chips may be used as well as synthesisable IP core in FPGA (home made or commercial).

The interface to the sub-detector controller shall present the information to / from the ODE board in a “LHCb standard” way to be used by the middle and top levels of the LHCb ECS.

1.3 ODE processing section and ODE infrastructure

The ODE processing section in the counting room will be based on commercial boards and systems (e.g. - multiprocessor PC or VME boards with DSPs). The connection to the ECS will be provided via Ethernet and will not involve any hardware development. It will be used for software down loading and for monitoring of the ODE processing section performance.

The ODE infrastructure in the cavern (racks, crates, power supplies, etc.) must be also connected to the ECS. This interface will be similar to other vertex detector sub-systems, like vacuum, gas, high and low voltage, alignment, etc. It might exploit industrial-like approach to interface to the ECS using PLCs and field-bus to connect sensors to the ECS sub-detector controller.

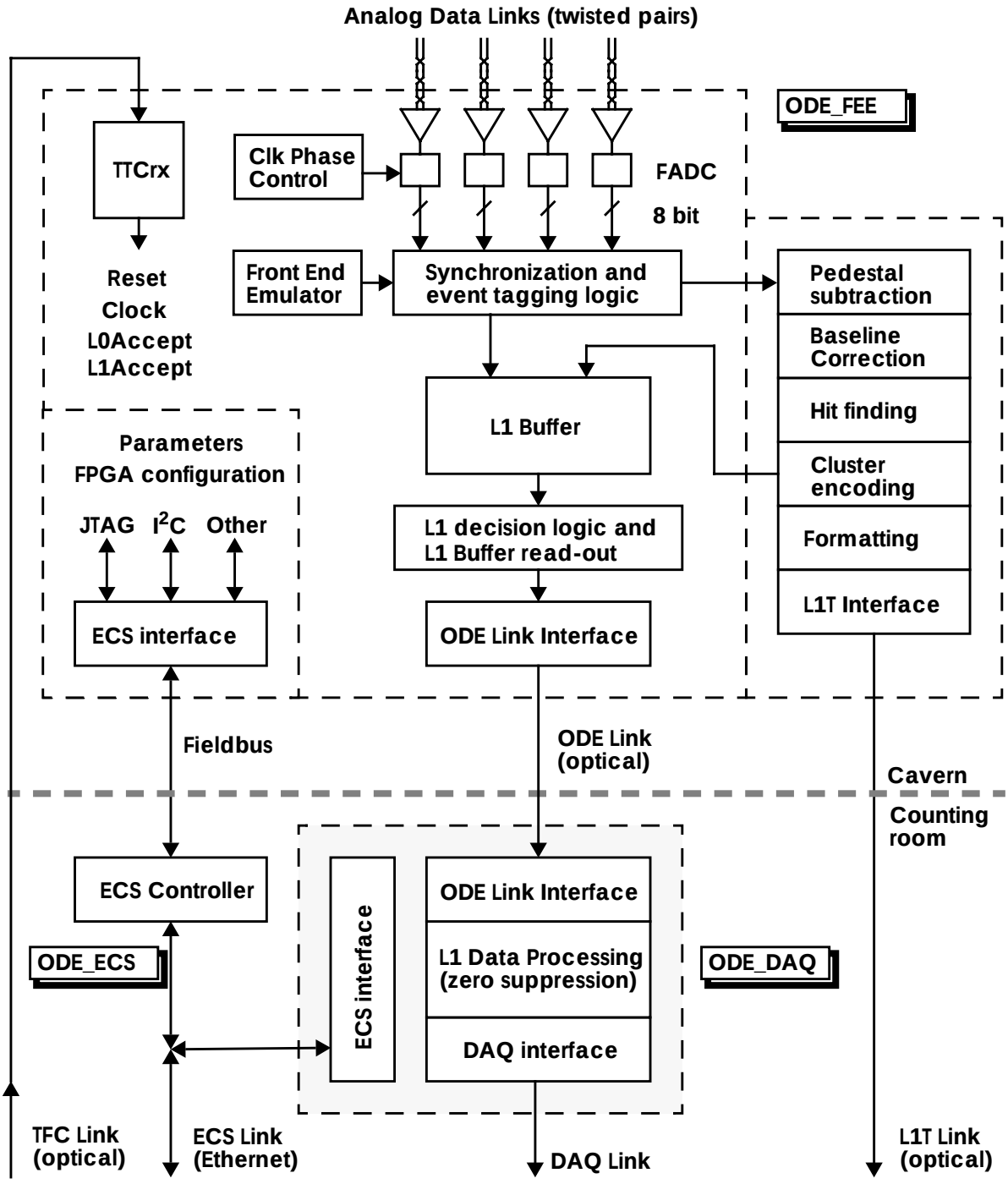

Figure 1. Vertex Detector Off-Detector Electronics

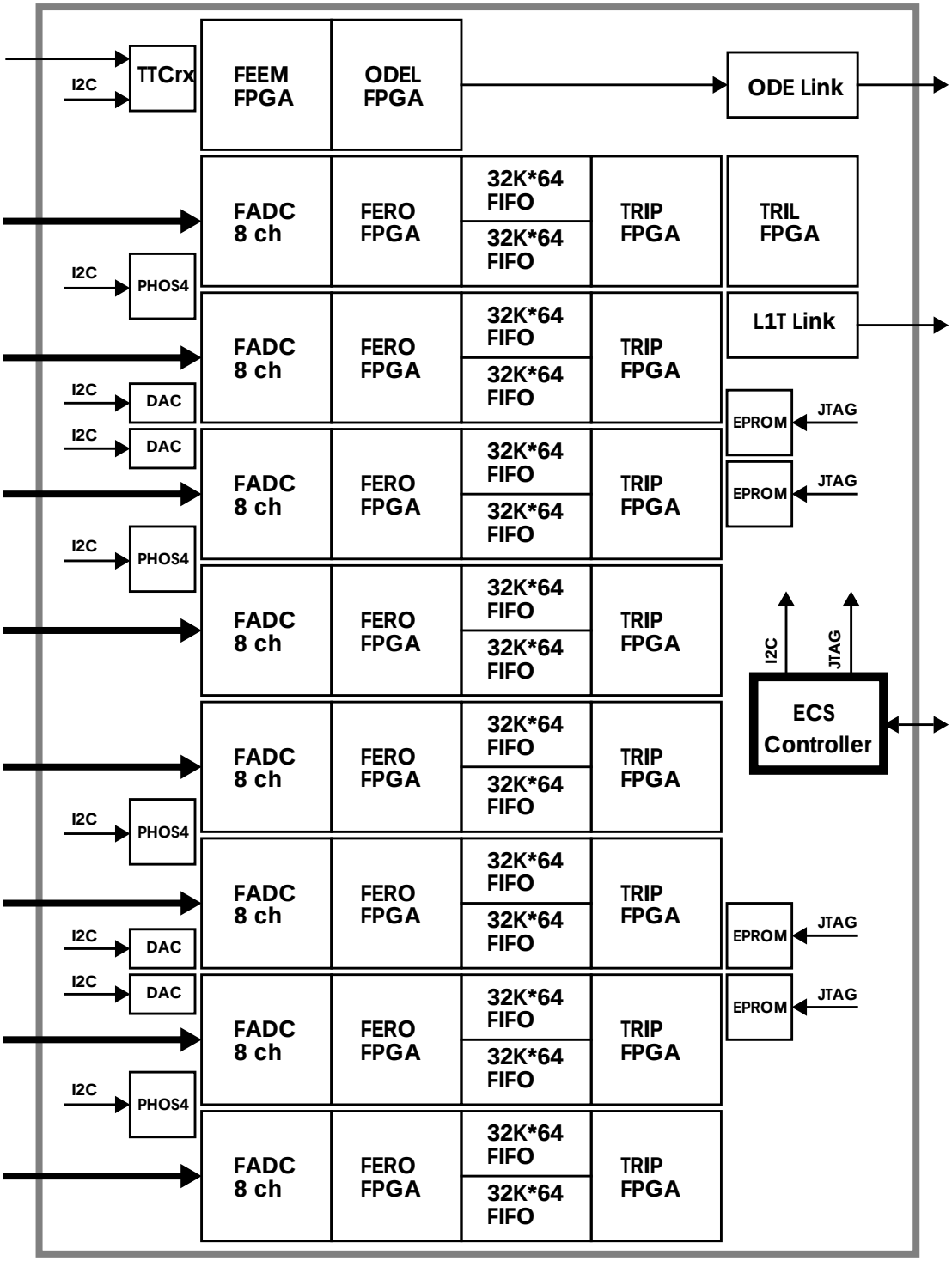

Figure 2. ODE 64-channels board

2 ODE on-board data access

Each ODE board processes 2K detector channels. It receives the analog multiplexed data from 64 input twisted-pair links (32 analog samples plus event identification per event), performs analog data digitizing using 8-channels FADC card with adjustable voltage reference (DAC) and clock phase (PHOS4).

FERO FPGAs performs synchronisation tasks and controls data storage in the L1 FIFO buffer using information from the TTCrx chip and the front-end emulator (FEEM). For accepted by the L1 trigger system events, non zero-suppressed data are collected from the L1 buffer and transferred to the processing section of the ODE in the counting room via ODE link under control of the ODEL FPGA.

The TRIP FPGAs perform data preprocessing for the L1 trigger system (pedestal subtraction, baseline correction, hit finding and cluster encoding). Formatted data are sent to the L1 trigger via L1T link under control of the TRIL FPGA.

2.1 ODE board registers

The registers on the ODE board are located inside different FPGAs and in the other components - TTCrx chip, programmable delay chip, digital-to-analog converters (DAC). They could be accesses using an uniform interface.

2.1.1 FADC reference voltage registers

One 8-bit (?) reference voltage register (plus DAC) is used for a group of 4 FADCs digitizing input analog data from one front-end chip. There is 16 registers in total on the ODE board. They could be implemented in the FERO FPGAs - 2 registers in each. The I2C interface can be used to read and write the registers using two I2C addresses. The DACs are outside of the FERO FPGA.

The other possible solutions are to use DAC chips with build-in I2C interface (e.g. AD5305 form Analog Devices - four 8-bit DACs in 10-pin package - 4 chips in total per ODE board) or one 16-channels DAC chip per ODE board (e.g. AD8600 from Analog Devices) with parallel interface [3].

2.1.2 FADC clock phase adjustment registers

One programmable delay line is used for a group of 4 FADCs digitizing input analog data from one front-end chip. There is 16 delay lines in total on the ODE board. They may be implemented using PHOS4 chip - 4 channel delay generation ASIC with 1 ns resolution (CERN microelectronics group development [4]) - 4 chips in total. The possible usage of commercial delay chips or custom delay line implementation using FPGA may be also considered. The PHOS4 chip provides 4 calibrated delay lines for digital signals, which can be programmed independently using 4 internal 5-bit delay registers accessible via the I2C

interface. The I2C access to each delay register is performed in one I2C data transfer. The 8-bit data word is divided into two sections: the upper 3 bits select one of the delay registers, the lower 5 bits specify the delay value. Of the 7 device address bits (A6..A0) four bits (A5..A2) correspond to the hard-wired device address, A6 is supposed to be zero and A1 and A0 are ignored. Four PHOS4 chips on the ODE board use four I2C addresses (out of 64).

2.1.3 TTCrx chip internal registers

The TTCrx chip [5] contains a total of 20 user-accessible 8-bit registers. The I2C interface is used to read and write (or reset) all the registers. After a write access, the corresponding register is, in general, set to the value of the transmitted data byte, however, writing into one of the counter registers resets it.

All data transfer over the I2C bus is performed using only two I2C registers: the I2C_pointer register and the I2C_data register. The I2C_pointer register is 5 bits wide and contains the address of the internal TTCrx register as defined in Table 3. The I2C_data register is used to read or write data from / to the internal TTCrx register, addressed by the I2C_pointer register. Hence each I2C access is performed in two steps: write the TTCrx internal register number in the I2C_pointer register and then read or write the I2C_data register.

The I2C_pointer and I2C_data registers occupy two consecutive positions in the 7 bit I2C address space. The upper 6 bits of the 7 bit I2C address are defined in the TTCrx ID_I2C<5:0> base address register and are initialised during a reset. One TTCrx chip on the ODE board uses two I2C addresses (out of 64).

2.1.4 FE emulator registers

The front-end emulator on the ODE board (FEEM FPGA) shall generate a predicted 8-bit pipeline number of the front-end chip for error detection purposes. It also contains 32-bit wide event counter (incremented by the L0Accept and set to zero by EvCntRes signals from the TTCrx chip) and 4-bit (?) input link delay register. The I2C interface can be used to read and write (or reset) all the registers. An implementation has to be defined (two I2C registers, like TTCrx chip - pointer / data for indirect access or three I2C registers for direct access).

2.1.5 Detector channel mask

Data from each individual detector channel can be disabled (set to zeros) using 1-bit mask register (2K in total). They can be grouped in 8-bit registers - 256 in total and implemented in FERO or TRIP FPGA - 32 8-bit mask registers per FPGA. The I2C interface can be used to read and write the registers using two I2C registers: the I2C_pointer register and the I2C_data register, similar to the TTCrx chip. The I2C_pointer register is 5 bits wide and contains the address of the mask register. The I2C_data register is used to read or write data from / to the mask register, addressed by the I2C_pointer register.

2.1.6 Hit threshold registers

There is one threshold register per TRIP used to store hit finder threshold - 8 in total per ODE board. Inside the TRIP the same threshold is used for all input links. The I2C interface can be used to read and write this register in TRIP using one I2C address.

2.1.7 Error statistics

There are an error detection circuits on the ODE board - one for each 4 input links from one front-end chip, 16 in total, implemented in the FEROs. Upon detecting an error (wrong event identification from the front-end electronics) the data for that event are disabled (set to zero) for the Level-1 trigger preprocessing and error flag for that event is written into the Level-1 buffer. The errors could be counted (e.g. 8-bit using counters or longer) and read periodically by the ECS. There are 16 (8-bit or longer) counters in total on the ODE board, two per FERO. The I2C interface can be used to read and reset these counters using two I2C addresses.

2.1.8 Run control register.

There is a run control register (8-bit ?) - one per board which defines the ODE board mode of operation. It could be implemented in the ECS interface or in one of FPGAs (e.g. ODEL or FEEM). The possible modes are: normal run (data from the front-end electronics), test run (data from the internal test memories).

2.1.9 Registers summary

Table 1

ODE registers	Total number	Data size (bit)	Location	Number	Registers per location	Access type	Access registers
FADC Vref	16	8	FERO / DAC	8 / 4	2 / 4	I2C	2*8 / 1*4
FADC clk	16	5	PHOS4	4	4	I2C	1*4
TTCrx	20	8	TTCrx	1	20	I2C	2
FEEM	3	4(?), 8, 32	FEEM	1	3	I2C	2
Ch. mask	256	8	FERO / TRIP	8	32	I2C	2*8
Thresholds	8	8	TRIP	8	1	I2C	1*8
Error	16	8	FERO	8	2	I2C	2*8
Run Ctrl	1	8	e.g. FEEM	1	1	I2C	uses FEEM
Total	338						64 / 52

2.2 ODE board memories

There are several memories on the ODE board - test memories, LUTs, Level-1 buffer. They are all read / write accessible from the ECS.

2.2.1 Input test memory

Each input link has it's own 256*8 FIFO test memory to emulate data from the front-end electronics and test the ODE in stand-alone mode. They are implemented inside the FERO

using internal memories in the FPGA - 8 FIFOs in total per FERO.

The I2C interface can be used to read and write FIFOs using two I2C registers: the I2C_pointer register and the I2C_data register, similar to the TTCrx chip. The I2C_pointer register is 3 bits wide and contains the address of the FIFO data / status registers. The I2C_data register is used to read or write data from / to the FIFO, addressed by the I2C_pointer register. The status register provides the access to the FIFO status - empty and full.

2.2.2 Pedestal LUTs

The pedestals (one per detector channel), which are used during data preprocessing for the L1 trigger system, are kept in the Look-Up Tables (LUT). There is one LUT (32*8) per input link, 64 LUTs in total per ODE board which corresponds to 2K*8 total LUT size. They are located inside TRIP FPGAs - 8 LUTs per TRIP. The pedestal values are calculated in the ODE processing section and loaded in the LUTs.

The I2C interface can be used to read and write LUTs using two I2C registers: the I2C_pointer register and the I2C_data register, similar to the TTCrx chip. The I2C_pointer register is 8 bits wide and contains 3-bit address of the LUT inside TRIP and 5-bit address of the data in the LUT. The I2C_data register is used to read or write data from / to the LUT, addressed by the I2C_pointer register.

It takes 4096 I2C transfers in order to down load all LUTs on the ODE board using individual addressing or 2056 I2C transfers using auto-increment addressing which corresponds to 100-200 ms using 400 kHz I2C clock frequency.

2.2.3 L1 buffer access registers

Digitized data from the front-end electronics and the data which are sent to the L1 trigger are stored on the ODE board in the L1 buffer during L1 latency - 1 ms. This required the L1 buffer capacity of 1000 events, which corresponds to (32K*8)*2 size of the buffer per input link - 4M*8 in total per ODE board. This buffer is implemented using FIFO memories (e.g. 32K*18 SyncFIFO - Cypress CY7C4275 [6] - 64 chips in total).

Interface to the FIFO data / status registers may be implemented using I2C interface, however it may take up to 200 s (~ 4 minutes) to dump the L1 buffer via 400 kHz I2C interface.

2.2.4 Memories summary

Table 2

ODE memory	Total number	Data size (bit)	Location	Memories per location	Access type	Access registers
Test memory	64	256*8	FERO	8	I2C	2*8
Pedestal LUTs	64	32*8	TRIP	8	I2C	2*8
L1B	64	(32K*8)*2	FIFO	-	?	
Total						

2.3 FPGA configuration

SRAM based FPGA requires configuration data to be loaded every time the circuit powers up. They can be loaded using configuration device, intelligent controller or the JTAG port [7]. For Altera FLEX 10K FPGA the configuration data sizes vary from 0.3 to 3.3 Mbit and for APEX 20K - from 1to 12 Mbit. For Altera FLEX EPF10K250A FPGA (3.3 Mbit of configuration data) the entire configuration process takes 320 ms with a clock frequency of 10 MHz.

FPGAs on the ODE board can be configured in different ways:

- From a configuration devices on the ODE board after power-up using FPGA configuration pins. The configuration device may be reprogrammed directly on the ODE board via built-in (JTAG) interface. The configuration device reprogramming is done using the ECS interface on the ODE board which has to have the JTAG master capability.
- From the memory of an intelligent ECS interface on the ODE board using FPGA configuration pins or using built-in JTAG interface in FPGA. The ECS interface shall provide control signals.

The above methods may be used together allow the maximum flexibility. The JTAG interface in the ECS controller may be used for boundary-scan testing, FPGA configuration and configuration device reprogramming. FPGA may be configured from both the configuration device via configuration pins and using built-in JTAG interface. The intelligent ECS controller shall have sufficient memory to store the configuration data.

2.3.1 Configuration devices

For Altera FLEX and APEX FPGAs two configuration devices can be used:

- EPC1 - one-time programmable, 1.1 Mbit EPROM in 8-pin PDIP or 20-pin PLCC package.
- EPC2 - 1.7 Mbit device with re-programmable (up to 100 times) FLASH configuration memory in 20-pin PLCC or 32-pin TQFP package, in-system programmability (ISP) through the built-in JTAG interface.

The largest APEX FPGA EP20K1500E needs eight EPC2 configuration devices.

2.3.2 JTAG programming

The built-in JTAG interface in Altera FPGA and configuration devices may be used to shift configuration data into FPGA and to re-program the configuration devices. This needs an intelligent ECS controller on the ODE board which uses the Jam programming and test language. Jam files contain both the programming algorithm and data and provided by the Altera development tools (Quartus and MAX+PLUS II).

3 ODE to ECS interface

Each ODE board will have an interface to the ECS sub-detector controllers. This interface (on-board ECS controller) shall provide an access from the ECS sub-detector controller to the internal ODE board resources. It has to interact from one side with the components on the ODE board and from the other side with the ECS sub-detector controller.

3.1 Internal ODE board interfaces

The internal ODE board interfaces shall provide an access to the commercial chips, FPGAs and memories on the ODE board from the on-board ECS controller.

3.1.1 I2C interface

The ODE board will need the I2C interface [1] on the board to access the internal registers in the DAC, PHOS4 and TTCrx chips where this interface is already built-in. FPGA internal registers may also be accessed using I2C interface, which has to be implemented in FPGA (as a simple I2C slave interface).

For the more complicated I2C master interface (I2C controller) a commercial chip could be used, e.g. is PCF8584 I2C-bus controller from PHILIPS [8]. There are several microprocessors with a built-in I2C controller, e.g. 80C51XA-based 16-bit micro-controllers from PHILIPS.

3.1.2 JTAG interface

The ODE board will need the JTAG interface [2] on the board to re-program configuration devices and optionally to configure FPGAs. The JTAG interface may be also used for boundary-scan testing of the ODE board.

3.2 External interface

The external ODE board interface (from on-board ECS controller to the ECS sub-detector controller) shall follow the recommendations of the LHCb ECS group. This could be either a field bus (e.g. CAN-bus [11]) or other serial bus (e.g. FireWire, [9], USB [10]) or Ethernet.

3.3 ECS controller on the ODE board

The ECS controller on the ODE board shall provide:

- An interface to the ECS sub-detector controller (e.g. FIreWire).
- I2C and JTAG interfaces to the components on the ODE board.
- Processing capability (CPU + memory).

The “ideal” solution would be a single chip controller with all these function, implemented on the chip.

4 References

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